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अभिरूचिकीअभिव्यक्ति/ EXPRESSION OF INTEREST

संदर्भ: एससीएल/61330/17/2019-20
Ref.: SCL/61330/17/2019-20 दिनांक/Dated: 03.01.2020

निदेशक, एससीएल के लिए एवं उनकी ओर से सेमी- कंडक्टर लेबोरेटरी (एसीएल) के प्रमुख क्रय एवं भण्डार, **'आरएफ डाउन कनवर्टर के डिजाइन एवं विकास हेतु बाहरी सेवाओं के लिए'** अभिरूचि की अभिव्यक्ति (EOI) आमंत्रित करते हैं।

For and on behalf of The Director, Head, Purchase & Stores, Semi-Conductor Laboratory (SCL) invites Expression of Interest (EOI) **for "External services for Design and Development of RF Downconverter ASIC."**

विवरण, योग्यता के नियम, चयनकी विधि एवं कार्य के परिक्षेत्र को EOI दस्तावेज में EOI प्रतिउत्तर फार्म में दर्शाया गया है, जो एससीएल की वेबसाइट (www.scl.gov.in/इसरो वेबसाइट(www.isro.gov.inपर उपलब्ध है एवं इसे वेबसाइट से भी डाउनलोड किया जा सकता है।

Description, Eligibility Norm, Selection Criteria & Brief Scope of Work etc. mentioned in the EOI document along with EOI Response Form is available at SCL website (www.scl.gov.in**)** /ISRO website (www.isro.gov.in) and the same can be downloaded from the website.

प्रश्न शीट के साथ अभिरूचि की अभिव्यक्ति बैठक में भाग लेने के इच्छुकों के लिए बैठक की तिथि एवं समय Date and time of submission of willingness to attend the Conference for EOI alongwith Query sheet over email	By 16.01.2020 **तक /** from 16:00 (IST)
अभिरूचि की अभिव्यक्ति बैठक की तिथि एवं समय Date and Time of Conference for EOI	23.01.2020 **को/** at 11:00 **बजे/** hrs (IST) onwards
अभिरूचि की अभिव्यक्ति मोहर बंद लिफाफे में प्रस्तुत करने की तिथि एवं समय Date & Time of Submission of Expression of Interest in Sealed Cover.	06.02.2020 upto 14:00 बजे/hrs (IST)

प्रमुख, क्रयएवंभंडारप्रभाग/Head, Purchase & Stores Division

Invitation for Expression of Interest (EOI)

Expression of Interest for Design and Development of RF downconverter ASIC

Semi-Conductor Laboratory (SCL) is engaged in Research & Development in the area of Microelectronics and MEMS. SCL has integrated facilities and supporting infrastructure for activities entailing Design, Development, Fabrication, Assembly & Packaging, Testing and Quality Assurance of CMOS and MEMS Devices for various applications.

SCL intends to seek services of competent design house/vendors, having adequate expertise in the design and successful delivery of RFIC (Radio frequency integrated circuit) products in CMOS technology. A tendering process shall be undertaken subsequently and short listed vendors only shall participate in this tendering process.

SCL solicits Expression of Interest (EOI) from Vendors interested in the Design and delivery of RF downconverter ASIC. The proposal should be submitted as an Expression of Interest (EOI), clearly indicating the expertise of the Vendor in RFIC design and successful delivery of RFIC products in CMOS technology. Company profile, areas of expertise and previous experience in this field should be clearly mentioned in the proposal.

1. Brief Scope of Work

Design, fabrication, packaging, testing, screening & qualification and delivery of RFIC receiver by the vendor as per following requirements.

1. To design RFIC receiver as per target specifications in Annexure-1.
2. Fabrication of the RFIC receiver after GDS tape-out in CMOS foundry.
3. Carry out packaging of RFIC dies.
4. Screening and qualification of final delivered devices.
5. To provide deliverables to SCL as specified in Annexure-2.

Detailed scope of work shall be mentioned in the RFP/tender to be issued subsequently to the short-listed vendors.

2. Eligibility Norm for the Bidder

1. Vendor(s) must have past experience of design and successful delivery of receiver in RFIC technology.
2. Vendor(s) should be a qualified/reputed RF VLSI design house who will undertake the design.
3. Vendor(s) shall have successfully completed design and GDS tape-out of atleast 3 RFIC products (transmitter/receiver/transceiver) for industrial applications during last 7 years. Vendor shall provide list of products and customer details to which RFIC products are delivered.
4. Vendor(s) shall provide supporting documents of having successfully designed and delivered RFIC receiver product to customer. Supporting document to be in form of customer acceptance, testimonial or data-sheet.
5. Vendor(s) responding to this EOI shall be short-listed based on an assessment of their capability and experience as mentioned above to undertake the proposed activities briefly mentioned under the head 'brief scope of work' in this document.

3. General Instructions for the submission of Expression of Interest (EOI)

1. The proposal should be submitted as an Expression of Interest (EOI), clearly Indicating the expertise and experience of the vendor in RFIC design and development.
2. EOI shall contain all the relevant details and supporting documents including references/ patents/data-sheets etc..
3. The request for EOI is not an offer and is issued with no commitment. SCL reserves the right to withdraw the request for EOI and change or vary any part thereof at any stage.
4. The shortlisted vendors shall be issued tender inquiry/Request for Proposal, inviting their technical and commercial bids at a later date.
5. SCL reserves the right to accept or reject all or any such Expression of Interest without assigning any reasons thereof.
6. SCL reserves the right to verify all claims made by the vendor.

4. Conference for the Expression of Interest

A conference for the Expression of Interest (EOI) may be arranged for prospective vendors in order to have a better understanding of our invitation for EOI document and to clarify doubts, if any. The interested vendors are hereby requested to take part in the conference for EOI on the Date & Time mentioned below:

Date & Time of submission of willingness to attend the Conference for EOI along with Query Sheet: 16th January 2020 upto 16:00 hrs (IST).

Query sheet should be sent at the following email IDs:

(i) dc@scl.gov.in
(ii) harjeet@scl.gov.in
(iii) abudhwar@scl.gov.in

Date & Time of EOI Conference for EOI: 23rdJanuary 2020 at 11:00 hrs (IST).

No queries shall be entertained after the Pre-Bid conference.

Date & Time of Submission of Expression of Interest in Sealed Cover: 6th February, 2020 upto 14:00 hrs(IST).

Your **Expression of Interest** should be sent **IN A SEALED ENVELOPE** superscribed with the Reference no. so as to reach SCL S.A.S. Nagar, Punjab on or before 6th February, 2020, by 14:00 hrs. (IST). **Please note that bid received over email/fax shall not be considered.**

Interested vendors may please provide the details of their representatives taking part in the conference for EOI well in advance. Vendor may participate in the EOI conference in person/ over telephonic conference/ over Skype. **The vendors who do not participate EOI Conference will not be eligible for participating in the bidding process.**

5. Indicative Milestones

As per Annexure–3.

6. Response Form

Vendors are requested to furnish the following details:

1.	Name and Address of the company: (Registered Office and Works) along with Phone, Fax, email and website.
2.	Year of establishment :
3.	Brief outline of the line of business and services offered:
4.	Details of the Management and Organizational Structure of the company:
5.	Total manpower (Break up on Managerial, technical and Auxiliary / Support Staff)
6.	Details of the Technical Team relevant to the proposed project:
7.	Details of Contract now in hand:
8.	Name and Address of Banker(s):
9.	Copy of Balance sheet for last three (3) years :

10.	List of product/services of similar kind provided earlier along with the list of customers or end users:
11.	Any other relevant information :
12.	Copy of Balance sheet, profit & loss account and latest income tax returns for last three years.
13.	List of similar contracts executed for the last three years with full address of customer and contact person (A copy of executed Purchase Orders/Contracts shall be enclosed)

We affirm that the information submitted is complete in all respects and true to the best of our knowledge and that we are authorized to submit this application. We understand that the information furnished in the form above is liable to be verified and any misrepresentation may lead to our disqualification from the tendering process.

Name of authorized signatory

Signature of the authorized signatory

Designation

Stamp

Date

Annexure -1

Features and Specifications

RF Down converter ASIC is required to down convert UHF (434MHz) to 10.7MHz Intermediate frequency(IF) using single stage down conversion super heterodyne architecture. The proposed ASIC is expected to provide constant amplitude IF over the specified range as provided in following functional requirement table. It is expected to meet IF rejection, spurious rejection, IF bandwidth requirements and provide RSSI signal (analog output) in 10.7MHz IF stage for monitoring. Built-in frequency synthesizer for LO generation is proposed.

Electrical specs:

Specification	Values	Remarks
Centre Frequency	434MHz	
Down Converted Frequency	10.7 MHz	50 ohm matched single ended output.
Input Impedance	50 Ω	Single ended
VSWR	1.5:1	RF input and IF output
Noise figure	2dB max	
Input dynamic range	-115dBm to -20dBm	
Mixer and LO generator	Mixer	Design parameters.[Note: Ref TCXO will be external to ASIC]
	RF: 100MHz to 500MHz	
	LO:100MHz to 500MHz	
	IF: DC to 500MHz	
	LO to IF isolation:20dBc	
	LO to RF isolation:25dBc	
	Synthesizer and VCO (External clock source with TTL or CMOS output will be provided for reference input).	
	VCO frequency: 100MHz to 500MHz	
	Freq Resolution :100Hz	

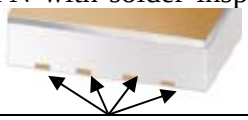
Specification	Values	Remarks
	Phase noise : 1kHz offset: -80dBc/Hz max 10kHz offset: -90dBc/Hz max 1MHz offset: -120dBc/Hz max	
	Reference TCXO (TTL/CMOS) spec: Frequency range : 10MHz to 40MHz. Stability: ±30ppm over -40°C to +85°C, Total Jitter : 50ps max	
Image Rejection	60dBc	45dBc min is required.
IF Rejection	80dBc min	
Filtering Rejection requirements from RF stage	434±10MHz: 20dBc min 434±21.4MHz: 45dBc min	
Spurious Response	Minimum 60dBc down except within 434±2MHz	
IF Bandwidth	IF Filter BW 3dB : 115kHz to 155kHz Linear phase response over the 3dB BW Rejection at fIF±2MHz: 60dBc	3dB BW value of 115kHz should be read as IF freq+/- 57.5 kHz.
IF Ripple	Less than 0.7dB	
IF Output level	Constant IF output over the input dynamic range of-115dBm to -20dBm.	Output at any level between -9 to -12 dBm but constant IF level (with tolerance of ±0.5 dB) is required.
10dB IF CNR point	-109dBm min	
AGC response Time	Stable AGC response desired. External capacitor provision may be provided to control response time.	Less than 1ms desired.
Received Signal strength Indicator	Output range : 0 to Vs for RF input: -115dBm to -20dBm	[Min required Linear RSSI range: -115dBm to -45dBm]
1dB gain desensitization	For out of band 434±10MHz: less than -30dBm	
Supply voltage	Vs±10%	Vs :+3.3V
Current	Probable current consumption can be indicated	Should be less than 150mA.
Input Power handling	0dBm max	

Pin Configuration :

S.No	Description	Name	Type	Function	Remarks
1.	RF Input	RF	RF	Input	-20dBm to -115dBm System should be able to handle 0dBm
2.	IF Monitoring O/P (After IF Bandlimiting)	IFM	RF	Output	Based on gain distribution (Can be indicated by party)
3.	Final IF output	IF	RF	Output	-9dBm to -12dBm (constant level±0.5dB)
4.	Signal Strength Monitoring	RSSI	DC	Output	0 to Vs for -115dBm to -20dBm RF input. Impedance<100 ohm is required.
Control signals for synthesizer/VCO					
5.	Serial clock	SCLK	Digital	Input	Serial Clock Input. This input is used to clock in the serial data to the registers 0/3.3V
6.	Data	SDATA	Digital	Input	Serial Data Input 0/3.3V
7.	Load Enable Input	LE	Digital	Input	0/3.3V
8.	MUX output	MUX	Digital	Output	0/3.3V Multiplexer Output. This pin allows various internal signals to be accessed externally depending on ve- - ndorconfiguration and choice. Vendor may clearly specify the signals.
9.	Reference Input for synthesizer TTL/CMOS Crystal Oscillator[10MHz to 40MHz external TCXO]	Ref in	Digital	Input	0/3.3V
10.	Lock Detect	LD	Digital	Output	0/3.3V Lock : 0V, unlock:3.3V
11.	Power Supply	Vs	DC	Input	3.3V
12.	Ground	Gnd	Gnd	Gnd	
13.	Charge pump out	CP_out	analog	output	Input to external loop filter
14.	VCO tuning input	V_tune	analog	input	Control input to VCO from

					external loop filter
15.	AGC time constant	AGC_TC	analog	output	Pin to connect external capacitor to adjust AGC time constant.

Mechanical specification:

S. No.	Description	
1.	Packaging	Ceramic QFN with solder inspect ability on all pins as indicated . 
2.	No. of Pins	Minimum15 as per pin configuration requirements
3.	Dimension	< 9mm x 9mm
4.	Bottom exposed paddle	To be provided for grounding and thermal management
5.	Hermetic Sealing	Required

Annexure-2

Deliverables to SCL and other items

S. No	Specification	Vendor Compliance (Yes/No)	Remarks
1.	Known good dies– 20nos.		
2.	Packaged devices-130 nos.		
3.	ASIC evaluation board/hardware along with required software – 5nos.		
4.	Packages without dies-20Nos		
5.	Sockets for testing (Quote to be given with slabs of 1-10Nos, 11-30Nos, 31-60Nos)		
6.	ASIC Evaluation Report and Datasheet		
7.	ASIC design GDS		
8.	Circuit schematic/netlist (Open access format)		
9.	Simulation test-benches and results		
10.	Design documentation of ASIC design including simulation test-benches, simulation and verification results of various sub-blocks and top-level ASIC.[As per section-6.2 in this document].		
11.	Silicon test results including functional on-wafer and package level testing results.		
12.	Vendor to provide screening and qualification results.		
13.	Vendor to provide SCL with PCM data of fabrication lot provided by foundry.		

14.	Perpetual, worldwide, royalty-free, sub licensable license for developed IP, to use, copy and modify the Developed IP for the purpose of having integrated circuits designed by, manufactured for, and sold under the name of SCL.		

Annexure-3

Delivery Period and Milestone Reviews

Milestone	Activity	Duration
1	Architecture design review	2 months
2	Circuit design and simulation and review	2 months
3	Backend design review	3 months
4	GDS-II tapeout , fabrication and Die level testing	3 months
5	Packaging and Prototype testing	1 month
6	Functional test, Screening and qualification, Design sign off	4 months