सेमी-कंडक्टरलेबोरेटरी/Semi-Conductor Laboratory
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अभिरूचिकीअभिव्यक्ति/ EXPRESSION OF INTEREST

संदर्भ: एससीएल/61328/17/2019
Ref.: SCL/61328/17/2019 दिनांक/Dated: 23.12.2019

निदेशक, एससीएल, प्रमुख, क्रय एवं भण्डार के लिए एवं उनकी ओर से सेमी- कंडक्टर लेबोरेटरी (एससीएल), सक्षम डिजाइन हाउस/विकसित करने वाले (वेंडरों), जिन्हें "एससीएल में 180nm सीमॉस प्रक्रिया FPGA अनुप्रयोग वातावरण EDA टूल्स के साथ FPGA चिप्स, रेडिएशन हार्डन्ड एवं नॉन रेडिएशन हार्डन्ड दोनों वर्जन में डिजाइन'' की उपयुक्त तकनीकी विशेषज्ञता प्राप्त हो, से अभिरूचि की अभिव्यक्ति (EOI) आमंत्रित करते हैं।

For and on behalf of The Director, Head, Purchase & Stores, Semi-Conductor Laboratory (SCL) invites Expression of Interest (EOI) from competent Design House/ Developers(Vendors), having adequate technical expertise in "Design of FPGA chips, both Radiation Hardened and Non-Radiation Hardened version, in SCL 180nm CMOS process along with FPGA application environment EDA Tools."

विवरण, योग्यता के नियम, चयनकी विधि एवं कार्य के परिक्षेत्र को EOI दस्तावेज में EOI प्रतिउत्तर फार्म में दर्शाया गया है, जो एससीएल की वेबसाइट (www.scl.gov.in/इसरो वेबसाइट(www.isro.gov.inपर उपलब्ध है एवं इसे वेबसाइट से भी डाउनलोड किया जा सकता है।

Description, Eligibility Norm, Selection Criteria & Brief Scope of Work etc. mentioned in the EOI document along with EOI Response Form is available at SCL website (www.scl.gov.in**)** /ISRO website (www.isro.gov.in) and the same can be downloaded from the website.

प्रश्न शीट के साथ अभिरूचि की अभिव्यक्ति बैठक में भाग लेने के इच्छुकों के लिए बैठक की तिथि एवं समय Date and time of submission of willingness to attend the Conference for EOI alongwith Query sheet over email	By 08.01.2020 **तक /** from 16:00 (IST)
अभिरूचि की अभिव्यक्ति बैठक की तिथि एवं समय Date and Time of Conference for EOI	15.01.2020 **को/** at 11:00 **बजे/** hrs (IST) onwards
अभिरूचि की अभिव्यक्ति मोहर बंद लिफाफे में प्रस्तुत करने की तिथि एवं समय Date & Time of Submission of Expression of Interest in Sealed Cover:	28.01.2020 upto 14:00 बजे/hrs (IST)

प्रमुख, क्रयएवंभंडारप्रभाग/Head, Purchase & Stores Division

Invitation for Expression of Interest

Design of FPGA chips, both Radiation Hardened and Non-Radiation Hardened version, in SCL 180nm CMOS process along with FPGA application environment EDA Tools

Semi-Conductor Laboratory (SCL), an autonomous body under Department of Space,Government of India, is engaged in Research & Development in the area of Microelectronics and MEMS. SCL has integrated facilities and supporting infrastructure for activities focused on Design, Development, Fabrication, Assembly & Packaging, Testing and Quality Assurance of CMOS and MEMS Devices for various applications.

SCL is looking for competent design house /developers (vendors), having sufficienttechnicalexpertise in **design** of FPGA chips along with FPGA application environment EDA tools. A tendering process for "**Design of FPGA chips, both Radiation Hardened and Non-Radiation Hardened version, in SCL 180nm CMOS process along with FPGA application environment EDA Tools**" with given Features and Specification as per annexure 1A shall be undertaken subsequently andshort listed vendors shall only be allowed to participate further.

SCL solicits Expression of Interest (EOI) from the vendors interested in the Design of FPGA chip and its associated design and application ecosystem. The proposal should be submitted asan Expression of Interest (EOI), clearly indicating the expertise of the vendor in the design and development of FPGA chip and its associated ecosystem. Company profile, areas ofexpertise and previous experience in this field should be included.

1. Scope of Work

Design of FPGA chips, both Radiation Hardened and Non-Radiation Hardened version, in SCL 180nm CMOS process along with FPGA application environment EDA Tools as per

- Features and Specification in Annexure 1A
- Deliverables to SCL and other items in Annexure 1B
- One Test chip fabrication and characterization for both non-RH and RH version prior to full and final non-RH and RH version FPGA chips fabrication for silicon validation is allowed based upon discretion of vendor
- Delivery Period and Milestone Reviews as per Annexure 1C

2. Eligibility norm for the Bidder

1. Parties responding to the invitation for EOI should have Office / Headquarter in India and having technical expertise in the design and development of ASIC / SOC / FPGA chip and its associated ecosystem. The bidder shall provide supporting documents/evidences for the same.

2. The design of FPGA chip and associated design and application EDA tools requires both Hardware and Software expertise. The Team leader(s) / Chief Architect(s) for this project - in both Hardware and Software domain – of the vendor shall have minimum Ten (10) years experience in the Design of FPGA chip at 180nm CMOS or better technology node and its associated design and application ecosystem / EDA Tools. The bidder shall provide supporting documents/evidences for the same for assessment of their eligibility.

3. Prospective parties should be able to provide evidence in support of having successfully delivered at least three (3) products of high complexity in form of ASIC / IP / SOC during the last three (3) years along with the list of customers. The bidder shall provide supporting documents/evidences for the same.

4. Prospective parties shall have IP rights of all modules, required to carry out proposed FPGA design. Prospective parties shall not use any third party IP used without proper authorization.

5. Prospective parties shall ensure availability of Team leader(s) / Chief Architect(s) responsible for the project for the entire duration of project.

3. General Instructions for the submission of Expression of Interest (EOI)

1. The proposal should be submitted as an Expression of Interest (EOI), clearly Indicating the expertise of the vendor in the design and development of FPGA chip and its associated design and application EDA tools.

2. EOI should contain all the relevant details and supporting documents including whitepapers and patents.

3. If required, the vendor responding to the EOI may be invited for further discussions at SCL for assessment of the capabilities stated in the EOI and for providing any clarifications.

4. The request for EOI is not an offer and is issued with no commitment. SCL reserves the right to withdraw the request for EOI and change or vary any part thereof at any stage.

5. The vendors shortlisted (based on EOI and assessment of their potential to carry out the proposed work) would be issued formal tender inquiry / Request for Proposal, inviting their technical and commercial bids at a later date.

6. SCL reserves the right to accept or reject all or any such Expression of Interest without assigning any reasons thereof.

7. SCL reserves the right to verify all claims made by the vendor.

4. Conference for the Expression of Interest

A conference for the Expression of Interest (EOI) may be arranged for prospective vendors in order to have a better understanding of our invitation for EOI document and to clarify doubts, if any. The interested vendors are hereby requested to take part in the conference for EOI on the Date & Time mentioned below

Date & Time of submission of willingness to attend the Conference for EOI along with Query Sheet:
08th January 2020 upto 16:00 hrs (IST)

Date & Time of Pre-Bid Conference for EOI:
15th January 2020 at 11:00 hrs (IST). No queries shall be entertained after the Pre-Bid conference.

Date & Time of Submission of Expression of Interest in Sealed Cover:
28th January 2020 upto 14:00 hrs(IST). Your **Expression of Interest** should be sent **IN A SEALED ENVELOPE** superscribed with the Reference no. so as to reach SCL S.A.S. Nagar, Punjab on or before 28th January, 2020, by 1530 PM (IST). **Please note that bid received over email/fax shall not be considered.**

Interested vendors may please provide the details of their representatives taking part in the conference for EOI well in advance. Vendor may participate in the EOI conference in person/ over telephonic conference/ over Skype. **The vendors who do not participate EOI Conference will not be eligible for participating in the bidding process.**

5. Response Form

Vendors are requested to furnish the following details:

1.	Name and Address of the company: (Registered Office and Works) along with Phone, Fax, email and website.
2.	Year of establishment :
3.	Brief outline of the line of business and services offered:
4.	Details of the Management and Organizational Structure of the company:
5.	Total manpower (Break up on Managerial, technical and Auxiliary / Support Staff)
6.	Details of the Technical Team relevant to the proposed project:
7.	Details of Contract now in hand:
8.	Name and Address of Banker(s):
9.	Copy of Balance sheet for last three (3) years :
10.	List of product/services of similar kind provided earlier along with the list of customers or end users:
11.	Any other relevant information :
12.	Copy of Balance sheet, profit & loss account and latest income tax returns for last three years.
13.	List of similar contracts executed for the last three years with full address of customer and contact person (A copy of executed Purchase Orders/Contracts shall be enclosed)

We affirm that the information submitted is complete in all respects and true to the best of our knowledge and that we are authorized to submit this application. We understand that the information furnished in the form above is liable to be verified and any misrepresentation may lead to our disqualification from the tendering process.

6. Intellectual property rights and Ownership

SCL shall hold all applicable Intellectual Property Rights for the architecture and design of the FPGA chips – both Non-RH and RH – and associated application EDA tools and SCL shall have the right to file applications for protection of the appropriate IP rights within India or Abroad at appropriate time related to this program. The vendor shall not claim any IP rights on design or manufacturing process involved in program.
The software and hardware developed under this program shall be the sole property of SCL. The vendor shall not have any right to reuse or modify the design of FPGA chips – both Non-RH and RH – and associated application EDA tools for any other purposes and shall not have any right to supply the same or similar or modified design of FPGA chips – both Non-RH and RH – and associated application EDA tools to any other customer(s), without the prior written permission from the competent authority at SCL.

7. Project Realization Flow

Vendor shall provide the project realization plan and methodology to SCL.

8. Payment Conditions

There will be provision for milestone based payments.

Name of authorized signatory

Signature of the authorized signatory

Designation

Stamp

Date

nnexure -1A

Design of FPGA chips, both Radiation Hardened and Non-Radiation Hardened version, in SCL 180nm CMOS process along with FPGA application environment EDA Tools

1. Features and Specifications of smaller FPGA

Features and Specifications as realized on silicon				
S. No.	Features and Specification	Smaller Non-RH	Smaller RH	Remarks
1	CLB (4 input LUT + DFF)	10K	10K	It may contain carry logic also depending upon vendor's architecture to cater ASIC gate (S. No. 2) specification or user defined
2	ASIC gate	≥ 100K	≥ 100K	
3	Clock Sources	Embedded PLL	Embedded PLL	
4	Core frequency	≥ 250 MHz	≥ 200 MHz	
5	SRAM Memory	≥ 100 Kbit	≥ 100 Kbit	Available for End User. Bit cell available at SCL
6	Total IO (Functional & P/G)	≤ 200	≤ 200	
7	Programmable GPIO (Functional)	≥ 120	≥ 120	Included in Total 200
8	IO standards	LVTTL, LVCMOS	LVTTL, LVCMOS	
9	IO Pads	Available in SCL	Available in SCL	
10	Package	208 pins	208 pins	
11	Process	180nm, 6 metal	180nm, 6 metal	
12	IO Supply	3.3V, 1.8V	3.3V, 1.8V	
13	Core Voltage	1.8V	1.8V	
14	Junction Temperature	-40 to 125 ℃	-40 to 125 ℃	
15	Anti-fuse (OTP)	Mature end of development at SCL	Mature end of development at SCL	
16	Die Area	≤ 6 mm x 6 mm	≤ 8 mm x 8 mm	
17	Configuration type	JTAG	JTAG	
18	Security	AES	AES	Advanced Encryption system
19	Embedded Multiplier	Yes	Yes	Fast multiplier (Specs TBD)
20	Testability	Yes	Yes	DFT and MBIST
21	Test Chip	No	No	Benchmarking

Vendor to provide line by line comments against the technical specifications, separately, for both non-RH and RH requirements provided by SCL in annexure 1.0. Vendor may bring out any other relevant technical specification not included in the above table.

Note : SCL will provide RH guidelines based upon its expertise along with RH bit cell and cell library.

2. Features and Specifications of Larger FPGA

Features and Specifications as realized on silicon				
S. No.	Features and Specification	Larger Non-RH	Larger RH	Remarks
1	CLB (4 input LUT + DFF)	40K	25K	It may contain carry logic also depending upon vendor's architecture to cater ASIC gate (S. No. 2) specification or user defined
2	ASIC gate	≥ 400K	≥ 300K	
3	Clock Sources	Embedded PLL	Embedded PLL	
4	Core frequency	≥ 350 MHz	≥ 300 MHz	
5	SRAM Memory	≥ 300 Kbit	≥ 150 Kbit	Available for End User. Bit cell available at SCL
6	Total IO (Functional & P/G)	≤ 500	≤ 500	
7	Programmable GPIO (Functional)	≥ 200	≥ 200	Included in Total 500
8	IO standards	LVTTL, LVCMOS	LVTTL, LVCMOS	
9	IO Pads	Available in SCL	Available in SCL	
10	Package	300 pins	300 pins	
11	Process	180nm, 6 metal	180nm, 6 metal	
12	IO Supply	3.3V, 1.8V	3.3V, 1.8V	
13	Core Voltage	1.8V	1.8V	
14	Junction Temperature	-40 to 125 ℃	-40 to 125 ℃	
15	Anti-fuse (OTP)	Mature end of development at SCL	Mature end of development at SCL	
16	Die Area	≤ 10 mm x 10 mm	≤ 15 mm x 15 mm	
17	Configuration type	JTAG	JTAG	
18	Security	AES	AES	Advanced Encryption system
19	Embedded Multiplier	Yes	Yes	Fast multiplier (Specs TBD)
20	Testability	Yes	Yes	DFT and MBIST
21	Test Chip	Yes	Yes	Benchmarking

Vendor to provide line by line comments against the technical specifications, separately, for both non-RH and RH requirements provided by SCL in annexure 1.0. Vendor maybring out any other relevant technical specification not included in the above table.

Note : SCL will provide RH guidelines based upon its expertise along with RH bit cell and cell library.

Annexure 1B

1. Deliverables to SCL

The following is list of deliverables to be provided by vendor to SCL. However, this list is not only limited to the following items and vendor may add any other item deemed relevant for successful execution of project.

1. DRC and DFM clean Fab-Ready GDSII
2. Physical Verification reports and database.
3. All source code (Verilog / VHDL / SPICE Netlist/layout database) and Soft IPs with perpetual license for unlimited use and modifications, transferred to SCL.
4. All Verification benches for hardware and software.
5. All Simulation results / waveforms.
6. Standalone binaries and GUI for FPGA application EDA tools.
7. Source code for generating end user tools: Standalone binaries and GUI for FPGA application EDA tools.
8. Any script used during build-up phase of FPGA
9. OS supported –RHEL 6 & above versions.
10. End-User FPGA kitalong with Hardware and Software details
11. FPGA board along with necessary interface / power cables for prototype device level testing for non-RH and RH
12. ATE test program and involvement of vendor engineer in wafer and packaged level testing of FPGA devices
13. Involvement of Vendor Team for Radiation Test for RH FPGA
14. Installations, Training and on-site Support for usage of both Software and Hardware delivered to SCL.
15. Detailed Know-how transfer to SCL, Documentation, Datasheet of entire design and all sub-modules.
16. Training for FPGA fabric flow with respect to scalability /upgradation
17. Milestone Reviews
18. Support for Two years after delivery of non-RH and RH FPGA kits.
19. Post warranty support of minimum 5 years of engagement with vendor
20. Design for benchmarking.
21. 50 number of end-user FPGA kit.

2. Responsibilities of SCL

As part of development of FPGA devices, SCL, apart from being involved in milestone reviews of activities, shall arrange for following:

1. SCL will provide 180 nm SCL PDK for both RH and Non-RH
2. Mask data preparation
3. Mask procurement
4. Fabrication for one test chip and one final chip for both RH and Non-RH version of FPGA.
5. Testing Facility (Wafer level and Packaged Device level)
6. Probe Card for Wafer-level Testing
7. Packages for few prototype samples
8. Radiation Testing
9. FM Screening and Qualification

Annexure 1C

1. Delivery Period

Vendor shall provide silicon proven FPGA devices along with all deliverables in full and final form as mentioned under deliverable to SCL as per following schedule

S. No.	Final FPGA Devices (Silicon Proven)	Delivery Time (months from placement of Purchase Order)*	Remarks
01	Non-RH (Smaller FPGA)	10	Test chip run included
02	Non-RH (Large FPGA)	16	No test chip run
03	RH (Smaller FPGA)	12	Test chip run included
04	RH (Larger FPGA)	18	No Test chip run

***Note:** This includes fabrication time of 3 months and 1 month for testing and packaging by SCL.

2. Milestone Review

During the development period of all FPGA devices – namely non-RH (smaller & larger) and RH (smaller & larger), SCL will conduct reviews of activities at following milestones:

1. Architecture Development
2. Pre-Layout sign off
3. Layout
4. Post Layout sign off
5. Silicon Validation