Record of clarification provided to the queries to the prospective bidders during Pre-Bid Meeting held at SCL on December 23, 2019 in response to the Public Tender Notice No. SCL/PT/163 (Tender No. SCL/PS2/2019E0158901) for External Design Service for Clock Generation Integer PLL IP.

1. Queries from M/s. Tecnode Solutions Pvt. Ltd., Bangalore, India (Attended via Skype)

Q1. Which process should the IP be designed for ? if it is SCL Process, will SCL Provide the PDK?
A1. SCL will provide SCL 180nm baseline process PDK for which vendor shall design the IP. Non-Disclosure Agreement shall be signed by the vendor for the SCL PDK.

Q2. How does SCL Plan to do the test chip?
A2. The design of test-chip for the demonstration of the PLL IP on the silicon is vendor's responsibility. The vendor is to share the test-plan and the test methodology.

Q3. Will SCL send the samples to the IP supplier (Rio System, Israel) OR do we need to send the PCB to SCL for testing?
A3. The dies shall be packaged by SCL in a mutually agreed package suggested by the vendor. Test/demonstration of the PLL IP on silicon will be performed by vendor at SCL premises. The vendor is to provide board (PCB) for testing and an on-site engineer to assist the testing procedures. Test-methodology and test-plan to be shared by the vendor.

Q4. Whether SCL will provide few samples of the device to vendor for debugging the board?
A4. SCL may send 5 numbers of packaged devices of the PLL test-chip to the vendor for board (PCB) debugging purposes. Approximately 25 numbers of PCB for testing shall be provided to SCL.

2. Queries from M/s. Risetime Semiconductors Pvt. Ltd., India(Attended via Skype)

Q1. The output frequency step is defined as 1MHz however input frequency is not defined. It may not be possible for input REFCLK frequencies other than 1MHz.
A1. The specification table along with output frequency step and output frequency dividers also defines input frequency divider range which may go upto 64. The vendor may thus use an input frequency which is at maximum 64 times the frequency required at the PFD input.

Q2. Clarifications are required for lock-to-lock and unlock-to-lock settling time.
A2. Lock-to-lock settling time means that once the PLL is in lock condition, any disturbance either on REFCLK or feedback divider, the time PLL takes to settle to new frequency must be less that 200us. Similarly, unlock-to-lock settling time means that from the time PLL is started (by powering it ON/Enable switch etc.), the time it takes to lock to the frequency must be less that 200us. The unlock-to-lock settling time specification may be also be considered for switching from test-mode to functional mode.

3. Queries from Sankalp Semiconductor Pvt. Ltd., India (Attended via Conference call)

Q1. Does the total jitter spec include random jitter (RJ) and deterministic jitter (DJ)?
A1. The total jitter specification includes both RJ and DJ. Both RJ and TJ (Total jitter) have been specified as upper maximum.

Q2. Can you please share BER target?
A2. Both Random jitter and Total jitter have been separately specified. Vendor may choose BER so as to meet these specifications.

Q3. Is there a BG reference design available at SOC level?
A3. Yes, BG reference is available at SOC level. However, SCL will not provide the BG reference IP to any vendor.

Q4. If yes what is the precision of outputs available from Band Gap reference?
A4. BG reference of 8-bit accuracy is available with SCL. However, SCL will not provide the BG reference IP to any vendor.

Q5. Can the PLL design assume to receive the required reference as inputs from Band Gap reference?
A5. SCL assumes BG reference to be part of the PLL IP to be provided by the vendor and will not share its BG reference IP to any of the vendors.

Q6. Can SCL provide feedback on our proposals and design reviews within a week for timely decision making?
A6. Review time is strongly dependent on the inputs provided by the vendor to the SCL team. Further, the schedule of the review meetings should be informed well in-advance to SCL so as to reserve the required time-slot. Given the proper inputs, SCL expects a maximum of 10 days for the feedback.

Q7. Does vendor completely own bring-up and bench testing of PLL or supports the debug ?
A7. Bench-testing shall be responsibility of the vendor. Only packaging and die assembly shall be provided by SCL on mutually agreed package.

Q8. Which package is planned for testing PLL and the final Product that includes the PLL?
A8. PLL may be packaged in mutually agreed package suggested by vendor. PLL can be tested/demonstrated on silicon separately as test-chip. However, support will be required for integrating PLL within an SOC.

Q9. Is Board designed by Customer or Vendor ?
A9. Testing board shall be designed and delivered by vendor.

Q10. Is it complete chip and package only for PLL test; will other SOC functions be disabled for PLL test ?
A10. A separate test-chip may be planned for demonstration of PLL on silicon.

Q11. Is SCL ready to share how to disable or not bond-out the other pins for SOC in case of test board is for PLL only?
A11. A separate test-chip may be planned for demonstration of PLL on silicon.

Q12. If all pins of SOC have to be bonded out please give description and count of pins to support the same for board design and testing?
A12. A separate test-chip may be planned for demonstration of PLL on silicon.

Q13. (i) Does the vendor needs to develop the testing software ?
(ii) If yes, is Labview the intended software for device level testing (Or please give details on

expected software)?

A13. Vendor shall demonstrate the silicon validation of the PLL IP fabricated at SCL. Vendor may choose either labview or custom test-plan/test-methodology to demonstrate the IP with all specifications.

4. <u>Queries from Moschip Technologies Ltd., Hyderabad, India(Attended in Person)</u>

Q1. Kindly let us know the % of tolerance in the jitter specs.

A1. The values defined in the specification table includes all tolerances.

Q2. SCL is looking for perpetual multi project(s) license?

A2. As per Clause No. 10 of “Item Specifications-I” of SCL’s Tender Document, PLL IP along with all the licenses shall be delivered to SCL for use without any royalty clause. SCL may use the IP as required in 'n' number of projects/products and 'n' number of times.

Q3. What is the programmability interface ?

A3. Any standard interface such as JTAG may be used by vendor. No custom or proprietary interface should be used.

Q4. Clause No. 13 of Item Specifications-I of SCL’s Tender Document: please explain in detail - ie mutually agreed

A4. Mutually agreement is referred in Clause no. 13 wherein mutually agreed testing methodology and mutually agreed package is to be worked out for testing of PLL. Please refer to Clause no. 13.

Q5. Number of PCB required by SCL?

A5. Approximately 25 numbers of PCB for testing shall be delivered to SCL.

Q6. Item specification: V - We assume our responsibility and payment will be received soon after completing the deliverables mentioned in the specifications, vendor payment will not be hold till SCL complete SOC and integration of this PLL - please clarify.

A6. SCL’s payment terms are clearly indicated in the ‘Vendor Specified Terms’.

Q7. Please clarify the applicability of the taxes.

A7. SCL shall issue Custom Duty Exemption Certificate, in case of Foreign supply or GST Exemption Certificate for indigenous supply for the deliverable goods. However, GST on service shall be payable at the rate of 18%. All payments shall be made after deduction of TDS as per Indian Law.

- Vendors expressed satisfaction on the response / clarifications provided to all the queries.
- The prospective bidders must take response / clarifications as recorded herein into account while submitting the bid to SCL.