



भारतसरकार/Government of India

अंतरिक्षविभाग/Department of Space

यू.आर. रावउपग्रहकेंद्र /U.R.RAO SATELLITE CENTRE

एच.ए.एल. एयरपोर्टरोड, विमानापुराडाक/HAL Airport Road, Vimanapura Post,

बेंगलूरु/BENGALURU – 560 017

Ref No.: ISMW 2025-0-67556

13.04.2026

**अंतरिक्ष VPX- आधारित समेकित उड्डयानिकी रैक-डेटा हस्तन तथा भंडारण प्रणाली के लिए इच्छा की अभिव्यक्ति (ई ओ आई)- के संबंध में।**

**Invitation for Expression of Interest [Eoi]**

**For Space VPX- based Integrated Avionics Rack-Data Handling and Storage System - Reg.**

अंतरिक्ष विभाग, भारत सरकार के अधीन भारतीय अंतरिक्ष अनुसंधान संगठन (इसरो) का यू.आर.राव उपग्रह केंद्र (यू.आर.एस.सी) (पूर्व में इसरो उपग्रह केन्द्र के नाम से विदित) सभी भारतीय उपग्रहों के अभिकल्प, विकास, संविरचन तथा परीक्षण के लिए उत्तरदायी है। वर्तमान में यू आर एस सी, अंतरिक्ष VPX-आधारित समेकित उड्डयानिकी रैक-डेटा उपयोग तथा भंडारण प्रणाली की आपूर्ति हेतु स्वदेशी उद्योग भागीदारों को आमंत्रित करता है।

U. R. Rao Satellite Centre [URSC] (Formerly known as ISRO Satellite Centre), of Indian Space Research Organization [ISRO] under Department of Space, Government of India is responsible for Design, Development, Fabrication and Testing of all Indian made Satellites. URSC is currently inviting indigenous Industry Partners for supply of Space VPX- based Integrated Avionics Rack-Data Handling and Storage System for space applications.

इस प्रस्ताव का उद्देश्य विशेष रूप से अंतरिक्ष VPX-आधारित समेकित उड्डयानिकी रैक-डेटा उपयोग तथा भंडारण प्रणाली की आपूर्ति हेतु तकनीकी अवसंरचना तथा क्षमता प्राप्त भारतीय उद्योगों से इच्छा की अभिव्यक्ति आमंत्रित करना है। ऐसे विक्रेता जो स्वीकार्य अंतरिक्ष VPX-आधारित समेकित उड्डयानिकी रैक-डेटा उपयोग तथा भंडारण प्रणाली की सुपुर्दगी करने हेतु इच्छुक हैं, इस प्रस्ताव का उत्तर दे सकते हैं। VPX-आधारित समेकित उड्डयानिकी रैक-डेटा उपयोग तथा भंडारण प्रणाली की आवश्यकताओं को इस दस्तावेज के अनुबंध के रूप में संलग्न किया गया है।

This proposal is to invite Expression of Interest exclusively from Indian industries having technical infrastructure and capability for supply of Space VPX- based Integrated Avionics Rack-Data Handling and Storage System. Those vendors which are interested to deliver the acceptable Space VPX- based Integrated Avionics Rack-Data Handling and Storage System may respond to this enquiry. The requirements of Space VPX-based Integrated Avionics Rack-Data Handling and Storage System are attached as Annexure to this document.



इस संबंध में, यू आर एस सी उन भारतीय उद्योगों/विक्रेताओं से इच्छा की अभिव्यक्ति (ई ओ आई) आमंत्रित करता है जो यू आर एस सी को स्वीकार्य अंतरिक्ष VPX-आधारित समेकित उड्डयानिकी रैक-डेटा उपयोग तथा भंडारण प्रणाली की सुपुर्दगी करने में सक्षम हैं।

In this regard, URSC invites the Expression of Interest [EOI] from Indian Industries/Vendors who have or are capable of delivering the acceptable Space VPX- based Integrated Avionics Rack-Data Handling and Storage System to URSC.

ई ओ आई का मूल्यांकन बोलीकर्ताओं के अनुभव, कार्यक्षेत्र की जानकारी, सुविधा अवसंरचना, प्रस्तावित कार्यप्रणाली और कार्य योजना, कुशल जनशक्ति और उद्योग की वित्तीय ताकत के आधार पर किया जाएगा।

The EOI will be evaluated on the basis of bidder's experience, understanding of scope of work, facility infrastructure, proposed methodology and work plan, skilled manpower and the financial strength of the industry.

यूआरएससी आवश्यकता पड़ने पर ईओआई की प्रक्रिया को रद्द करने/पुनः जारी करने या और जानकारी/विवरण मांगने का अधिकार सुरक्षित रखता है।

URSC reserves the right to cancel/re-issue the process of EOI if the necessity so arises or to seek further information/details.

यदि कोई कंपनी/फर्म किसी भ्रष्ट या धोखाधड़ीपूर्ण व्यवहार में लिप्त पाई जाती है, तो उसे निविदा प्रक्रिया में भाग लेने से रोक दिया जाएगा और उसके ईओआई दस्तावेज़ पर विचार नहीं किया जाएगा।

Companies/Firms, if found to have indulged in any corrupt or fraudulent practices, will be debarred taking part in the Tendering process and their EOI Document will not be taken up for consideration.

इच्छा की अभिव्यक्ति के साथ-साथ आपूर्तिकर्ताओं/फर्मों को निम्नलिखित जानकारी भी विस्तार से प्रस्तुत करनी चाहिए:

Along with "Expression of Interest" Suppliers/ Firm[s] should furnish the following information also in detail:

1. कंपनियों का पंजीकृत पता के साथ, फोन, फ़ैक्स, ईमेल, वेब आदि।  
Registered address of the Companies with Phone, Fax, Email, Web etc.
2. कंपनी/संगठन की स्थिति (स्वामित्व/साझेदारी/निजी/सार्वजनिक लिमिटेड आदि) के साथ मालिक, भागीदारों, निदेशक मंडल आदि के नाम और पता।  
Company/Organization Status (Proprietary/Partnership/Private/Public Ltd. etc.) with Name and Address of Proprietor, Partners, Board of Directors, etc.
3. सहयोगी: (ए) भारतीय (बी) विदेशी।  
Associates: (a) Indian (b) Foreign.
4. पिछले 3 वर्षों के दौरान प्रमुख ग्राहकों की सूची, पूर्ण पता और उनके संपर्क व्यक्ति।  
List of Major Customers during the last 3 Years with full address and their Contact Persons.
5. स्वामित्व वाली/उपलब्ध अवसंरचना सुविधाओं का विवरण।  
Details of Infrastructure Facilities owned / available.



6. कंपनी के प्रमुख शेयरधारकों के नाम और पते तथा उनकी शेयर पूंजी का प्रतिशत।  
Names and addresses of the major Shareholders of the Company and the percentage of their share capital.
7. नवीनतम वार्षिक रिपोर्ट की प्रति के साथ पिछले 3 वित्तीय वर्षों के लिए पूंजी और कारोबार।  
Capital and Turnover for the preceding 3 Financial Years with copy of latest Annual Report.
8. उपलब्ध वित्तीय क्षमता /क्रेडिट सुविधाएं।  
Financial Capacity/Credit facilities available.
9. बैंकों का नाम, पता व खाता विवरण।  
Name, Address of Bankers and Account details.
10. व्यापार संघ जिससे उद्योग जुड़ा/ जुड़े हैं।  
Trade Association to which Industry/ies belong to.
11. संस्था/बिक्री/माल व सेवा कर पंजीकरण संख्या।  
Establishment/Sales/Goods & Services Tax Registration Number and PAN details.
12. व्यापार का प्रकार।  
Nature of Business
13. कर्मचारियों की संख्या सहित संगठन की संरचना।  
Organization structure along with no. of employees.
14. बैंकों द्वारा जारी फर्म की सॉल्वेंसी/वित्तीय क्षमता।  
Solvency/Financial capacity of the Firm issued by their Bankers.
15. उद्योगों की अन्य कोई प्रासंगिक जानकारीयाँ।  
Any other information the Industry/ies consider relevant.
16. सामर्थ्य और कमियों के क्षेत्रों को स्पष्टतः प्रकट करते हुए कंपनी/कंपनियों के प्रोफाइल  
The Profile of the Company/ies clearly bringing out the areas of Strength and Weaknesses.
17. ई ओ आई में भाग लेने के लिए तकनीकी और संगठनात्मक सामर्थ्य का स्व-मूल्यांकन।  
Self-Assessment Technical and Organizational Competence to take part in the EOI.
18. ई ओ आई में उल्लिखित प्रत्युत्तर प्रपत्र  
Response forms as mentioned in the Eoi

### **ईओआई प्रतिक्रिया को पूरा करना/Completion of the EOI Response:**

- a) ईओआई दस्तावेजों के सभी अनुदेशों: निबंधन और शर्तों: प्रपत्रों: आवश्यकताओं और अन्य सूचनाओं का सावधानीपूर्वक अध्ययन करने की कंपनी/ फर्म को सलाह दी जाती है। ईओआई दस्तावेजों का सावधानीपूर्वक अध्ययन और जांच के बाद इसके निहितार्थों को पूरी तरह समझ कर ईओआई प्रस्तुत करना पड़ेगा।

The Company/Firms are advised to study all the instructions; Terms and Conditions; Forms; Requirements and other information in the EOI documents carefully. The submission of EOI shall be deemed to have been done after a careful study and examination of the EOI documents with full understanding of its implications.

- b) इस ई ओ आई का जवाब सभी मामलों में पूर्ण और संपूर्ण होना चाहिए। ई ओ आई दस्तावेज द्वारा आवश्यक सभी जानकारी प्रस्तुत करने में विफलता या ईओआई दस्तावेजों के हर पहलू के प्रति पर्याप्त रूप से उत्तरदायी न होने वाला प्रस्ताव प्रस्तुत करना, कंपनी/फर्म के जोखिम पर होगा और इसके परिणामस्वरूप दस्तावेज को अस्वीकार किया जा सकता है।  
The response to this EOI should be full and complete in all respect. Failure to furnish all the information required by the EOI document or submission of proposal not substantially responsive to the EOI documents to every aspect will be at the risk of the Company/Firms and may result in rejection of the document.
- c) प्रस्तुत किए गए ईओआई के सभी पृष्ठों पर क्रमांक होनी चाहिए और अधिकृत हस्ताक्षरकर्ता द्वारा हस्ताक्षरित होना चाहिए।  
All the pages of the EOI submitted must be numbered and signed by the authorized signatory.
- d) ई ओ आई के संबंध में प्रचार करना सख्त वर्जित है और एजेंसी द्वारा प्रस्तुत किए गए ऐसे प्रचारित ईओआई को अस्वीकार किया जा सकता है।  
Canvassing in connection with the EOI be strictly prohibited and such canvassed EOI submitted by the Agency are liable to be rejected.

क्रियाकलापों को अच्छी तरह समझने और यदि कोई संदेह हो तो उसका निवारण करने हेतु यू आर राव उपग्रह केन्द्र द्वारा एक पूर्व ई ओ आई बैठक का आयोजन किया जाएगा। तदुपरांत, आर एफ पी में मांगे गए विवरण के साथ विक्रेताओं को इच्छा की अभिव्यक्ति की प्रतिक्रिया प्रस्तुत करना होगा।

A Pre-Eoi meeting will be arranged by U.R. Rao Satellite Centre, Bengaluru in order to have a better understanding of the activities involved, clarify doubts, if any. Subsequently, the vendor(s) shall submit the response to Expression of Interest along with the details sought in RFP.

विनिर्दिष्ट दिनांक के पहले पूर्व बोली बैठक में भाग लेने वाले प्रतिनिधियों के विवरण सुरक्षा स्वीकृति का प्रबंध करने हेतु तालिका – 1 में विनिर्दिष्ट संपर्क व्यक्ति को कृपया उपलब्ध करें। विक्रेता के प्रतिनिधि को पूर्व ई – ओ आई बैठक में भाग लेने हेतु "प्राधिकार पत्र" लाना होगा। बोली लगाने वाले/कंपनी/संगठन से सदस्य प्रतिनिधि की संख्या अत्यधिक केवल दो (2) (एक तकनीकी तथा एक वित्तीय) तक सीमित होना चाहिए।

Interested Vendor[s] may please provide the details of the representative[s] taking part in the Pre-Eoi meeting well in advance prior to dates specified in Table-1 to the Focal Point in order to arrange for Security clearance. Vendor[s] representative shall carry an "Authorization Letter" for attending the Pre-Eoi meeting. Member Representative shall be limited to maximum of two (2) per bidder/ company/ organization.

विक्रेता द्वारा पूर्व ई ओ आई पूछताछ, पूर्व बैठक की दिनांक के 05 दिन पहले richa@ursc.gov.in को एक प्रति अंकित करते हुए यू आर एस सी की ई मेल आई डी pso\_f@ursc.gov.in पर पहुँचना चाहिए। कृपया नोट करें कि किसी भी परिस्थिति में, पूर्व ई ओ आई के लिए पूर्वन/स्थगन के अनुरोध पर विचार नहीं किया जाएगा।



Pre-EOI Queries from vendor [s] shall reach URSC 5 days prior to date of Pre-EOI meeting to e-mail ID: [ps0\\_f@ursc.gov.in](mailto:ps0_f@ursc.gov.in) marking a copy to [richa@ursc.gov.in](mailto:richa@ursc.gov.in) Please note that request for "Preponement/postponement of Pre-Eoi meeting" will not be entertained under any circumstances.

उपरोक्त सभी जानकारी के साथ इच्छा की अभिव्यक्ति नीचे दिए गए पते पर, उपरोक्त संदर्भ संख्या का उल्लेख करते हुए, नियत तिथि और समय तक पहुंच जानी चाहिए।

"Expression of Interest" with all the above information shall reach the address given below, quoting the above Reference Number on or before the due date & time.

वरिष्ठ प्रधान, क्रय एवं भंडार/Sr. Head, Purchase & Stores

यू आर राव उपग्रह केंद्र/U R Rao Satellite Centre,

एचएएल एयरपोर्ट रोड/HAL Airport Road,

विमानपुरा पोस्ट, बेंगलुरु/Vimanapura Post, Bengaluru, 560 017

कर्नाटक, भारत/Karnataka, India

कृपया ई ओ आई बैठक संख्या का उल्लेख करते हुए अपने स्पष्टीकरण [richa@ursc.gov.in](mailto:richa@ursc.gov.in) को अंकित करते हुए [ps0\\_f@ursc.gov.in](mailto:ps0_f@ursc.gov.in) मेल पर भेजें। पूर्व ई ओ आई बैठक में भाग हेतु अनुरोध 30.04.2026 (गुरुवार) 16:00 बजे या उससे पहले यहाँ उल्लिखित ई-मेल पर पहुँच जाना चाहिए। तथापि ई ओ आई का जवाब (हार्डकॉपी) केवल ऊपर उल्लिखित डाक पते पर ही भेजा जाएगा। ई मेल व फैक्स कोटेशन स्वीकार्य नहीं हैं। नियत तिथि और समय के बाद प्राप्त कोटेशन स्वीकार्य नहीं हैं।

Please address your clarifications quoting the EOI number to e-mail: [ps0\\_f@ursc.gov.in](mailto:ps0_f@ursc.gov.in) marking a copy to [richa@ursc.gov.in](mailto:richa@ursc.gov.in). Request for participation in Pre-Eoi meeting shall reach on or before 30.04.2026 (Thursday) 16:00 Hrs IST to the e-mail ids mentioned herein. However, response to EOI (hardcopy) shall be sent to above mentioned postal address only. E-mail & Fax quotations are not acceptable. Quotation received after due date & time are not acceptable.

### तालिका /Table 1:

Submission of EOI Details	
स्पष्टीकरण प्रस्तुत करने की अंतिम तिथि Last date of submission of Pre-Eoi clarification	30.04.2026 16:00 Hrs IST
प्री-ईओआई बैठक (PDMG सम्मेलन कक्ष, स्वगत कक्ष, यू आर एस सी में): Pre-EOI meeting (at PDMG Conference Hall, INSAT Building, URSC)	07.05.2026 10:00 Hrs IST
ईओआई प्रस्तुत करने की अंतिम तिथि	04.06.2026 13:00 Hrs IST



Last date for submission of EOI	
ई ओ आई की खुलने की तिथि Opening date of EOI	04.06.2026 14:00 Hrs IST

उपरोक्त सभी जानकारी के साथ इच्छा की अभिव्यक्ति **04.06.2026 13:00 बजे IST** तक या उससे पहले उपरोक्त संदर्भ संख्या का उल्लेख करते हुए, नीचे अधोहस्ताक्षरी को पहुँच जानी चाहिए। यह प्रस्ताव पूर्व-ईओआई अर्हता के रूप में आरंभ किया गया है। यूआरएससी बिना कोई कारण बताए सभी या किसी भी ऐसी इच्छा की अभिव्यक्ति को स्वीकार या अस्वीकार करने का अधिकार सुरक्षित रखता है।

“Expression of Interest” with all the above information shall reach the undersigned, Quoting above Reference Number on or before **04.06.2026 13:00 Hrs IST**. This proposal is initiated as a Pre-EOI Qualification. URSC reserves the right to accept or reject all or any such “Expression of Interest” without assigning any reasons what so ever.

इस ई ओ आई के लिए यदि कोई शुद्धिपत्र/अनुशेष हो तो इसे हमारे वेबसाइट [www.isro.gov.in](http://www.isro.gov.in) पर डाला जाएगा।

Addendum/Corrigendum, if any, to this Eoi, shall be hosted at our website, [www.isro.gov.in](http://www.isro.gov.in)

डिस्कलाइमर: इस आमंत्रण के अंग्रेजी और हिन्दी अनुवाद में विसंगति या असंगति यदि हो तो अंग्रेजी पाठ को सही माना जाएगा।

Disclaimer: The English version shall always prevail in case of any discrepancy or inconsistency between English and Hindi version of this Invitation.

Sd/-

**व. प्रधान, क्रय व भंडार/Sr. Head, Purchase & Stores**



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# Expression of interest for development of IAR-DHSS

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## 1 Introduction

The scope of this document is to provide the basic information related to Data Handling and Storage system (DHSS), and EOI process. It further specifies criteria for vendor selection.

URSC is seeking expressions of interest (EOI) from vendors to design and develop a SpaceVPX-based Integrated Avionics Rack-Data Handling and Storage System (IAR-DHSS) in 3U/6U form factors. Proposers must demonstrate technical expertise across the full development lifecycle—from initial block-level design and PCB layout to mechanical packaging, component procurement, and flight-model realization. The scope includes embedded software/IP core development, comprehensive verification and validation of throughputs, and the delivery of both prototype and flight-qualified hardware.

## 2 EOI process

Expression of Interest (EOI) for identifying suitable vendors for development of IAR-DHSS will have a Pre-EOI meeting where interested vendors will be briefed regarding the process as detailed in figure 1.

A detailed vendor selection criterion is provided in this document, for which prospective vendors are required to provide all the documentary proofs as per the list. All responses will be evaluated by URSC and a list of probable vendors will be selected.

Package specifications required to make a proposal is provided in this EOI. Based on the data, vendor is expected to give an engineering proposal with all technical details along with project execution plan. A presentation from vendor may be sought to understand the proposal.

All received proposals will be evaluated based on a pre-defined criterion mentioned in this document, and list of selected vendors will be generated. An indenting process will be initiated in a Limited tender mode only on those vendors whose EOI is selected. A flow chart of the process is as shown in Figure 1.

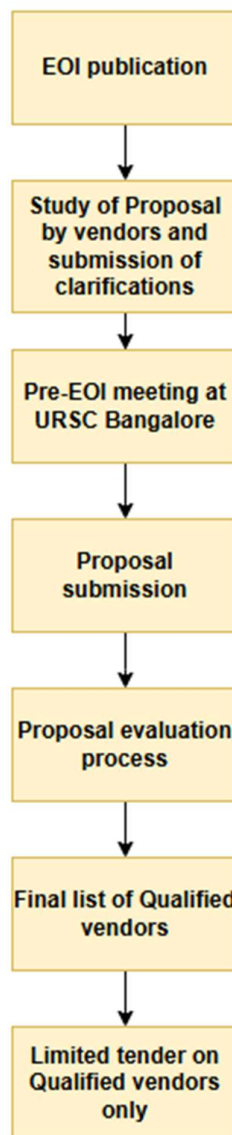


Figure 1: EOI process

### 3 Functional description of package

#### 3.1 Introduction

To meet the BAS requirements for Data Handling and Storage (DHSS) a modular, scalable and serviceable architecture has been envisaged with standard SpaceVPX based backplane. The proposed architecture consists of the following cards:

- Power module
- System Controller
- Payload Interface card/Data switch – 2 numbers
- Processing card/Inference card – 2 numbers
- Storage cards – 3 numbers

Each card dimension can be 6U or 3U, as required for accommodation of the necessary interfaces. The design must align with the provided architectural block diagram and strictly adhere to VITA 78 SpaceVPX standards for mechanical, electrical, and protocol compatibility.

NASA’s recommendations for SpaceVPX (<https://ntrs.nasa.gov/citations/20220013983> ) will be followed for interoperability and rapid deployment. Hence the following protocols shall be implemented on the different planes:

- Data Plane: Ethernet
- Expansion Plane: PCIe
- Control Plane: SpaceWire

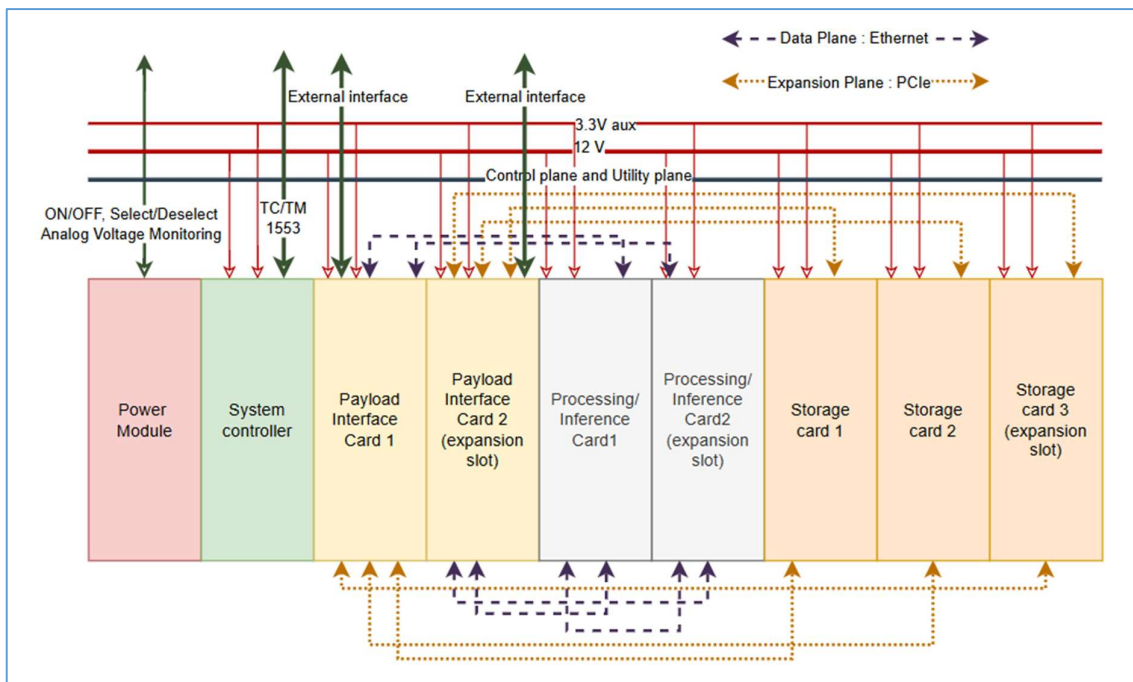


Figure 2: Data Handling and Storage system (DHSS) architecture(tentative)

### 3.1.1 Backplane-Profile

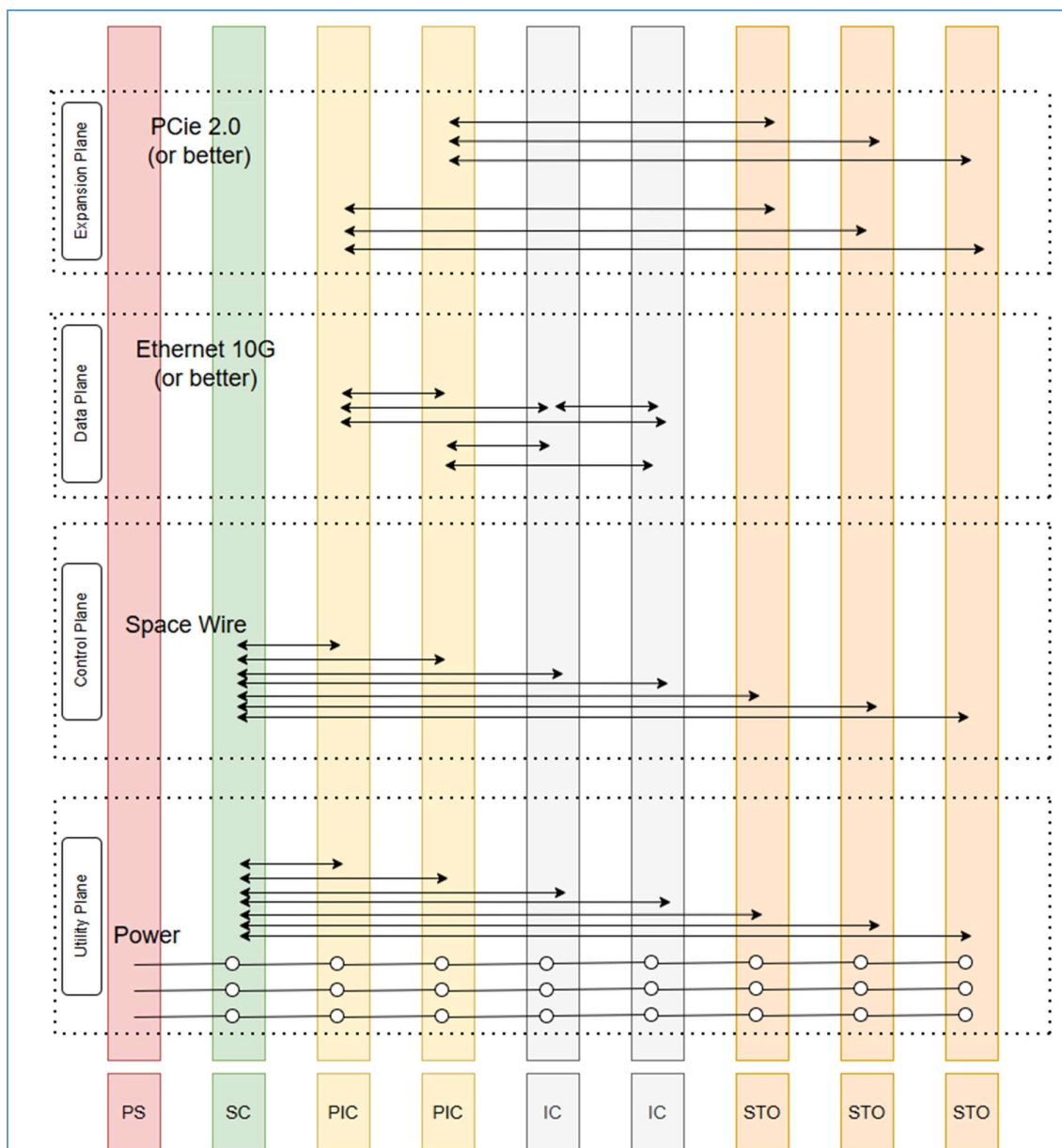


Figure 3: Backplane profile for IAR-DHSS (tentative)

PS : Power Supply  
 SC : System Controller  
 PIC: Payload interface card  
 IC: Inference card (/processing card)  
 STO : Storage card

### 3.1.2 Mechanical specifications for all the cards/package:

- **Form Factor:** The cards shall adhere to a 3U or 6U SpaceVPX (VITA 78) form factor.
- **Thermal management:** Conduction-cooled frame (VITA 48.2) design optimized for vacuum environments. Wedge-locks for thermal transfer to chassis rails.
- **Blind mating:** The mechanical design shall support blind mating of all cards into the backplane. External interfaces shall be provided through back fascia. Provisions shall be there for some external interfaces on the front fascia for Human-Machine Interaction (HMI) or debug purposes.
- **Component selection:** All components selected for the Prototyping (Proto) model must have a pin-compatible, space-grade equivalent available for the flight model.
- **Operating Humidity:** The system shall operate reliably in a Relative Humidity range of 30 to 70%.

### 3.1.3 Radiation Reliability Strategy in Flight model

- **Radiation tolerance** of space-grade components on the card for Flight Model:
  - **Total Ionizing Dose (TID):** 10 krad(Si) or better.
  - **Single Event Latch-up (SEL):** Immune upto a Linear Energy Transfer (LET) of 60 MeV-cm<sup>2</sup>/mg or better.
- **Radiation Mitigation Techniques:**
  - **SEU/SEFI Protection/process:** The solution must employ SEU (Single Event Upset) and SEFI (Single Event Functional Interrupt) mitigation techniques e.g. EDAC protected memories, scrubbing etc.

## 3.2 Brief introduction of cards:

### 3.2.1 Power Supply Card

The Power Supply Card (PSC) houses a high-efficiency radiation-hardened isolated DC-DC converter generating backplane supplies from Satellite Raw bus of 100V, designed to power the entire SpaceVPX chassis. The design shall adhere to VITA 78 (SpaceVPX) mechanical and electrical specifications.

**Secondary Power requirement:** ~220W

Input Signals:

*Table 1: Power supply card - Input signals*

<i>Sl No</i>	<i>Description</i>	<i>Remarks</i>
1.	Satellite Bus Voltage	100V ±3 V
2.	Discreet commands (5V,64ms) OPTO-ISOLATION	5V CMOS lines for ON 5V CMOS lines for OFF 5V CMOS lines for SELECT 5V CMOS lines for DESELECT

## Output Signals:

Table 2: Power supply card - Output signals

Sl No	Description	Remarks
1.	Backplane +12V – Main 1 (can be multiple switched outputs)	16A
2.	Backplane +5V – Main 2 (optional)	3A
3.	Backplane 3.3V AUX (unswitched)	3.3V @ 3A
4.	Bit monitoring	Power supply card On /off status for all the output voltages
5.	Analog Voltage Monitoring	For all output voltages
6.	Thermistor monitoring	10k thermistor (2 nos.)

### Features:

- Compliance to SpaceVPX (VITA 78.1-2022), MIL-STD-461 (EMI/EMC)
- Load regulation  $\pm 1\%$
- Isolation between Primary (Input) and Secondary (Output/Chassis) grounds.
- UVLO- Undervoltage lockout, Over-voltage Protection (OVP), Over-current Protection (OCP) capability

### 3.2.2 System Controller

The System Controller Card in a SpaceVPX (VITA 78) architecture is the "anchor" of the chassis. The System Controller is the primary bridge between the spacecraft's On-Board Computer (OBC) and the internal high-speed cards. It communicates with OBC for TM/TC exchange, Auxiliary (Aux) data for storage and downlink, PPS signals for time synchronization. It has the provision for global reset of all the boards through an OBC discrete command or a selective card reset. It is also responsible for the Health & Fault Management of the cards. It shall monitor the voltages, temperatures, currents and heart-beat signals from various cards and take appropriate actions as per the FDIR requirements

Power Budget= ~10W.

### Interfaces:

- **External Interfaces:**
  - **MIL-STD-1553B** with OBC for TM/TC and Aux data transfers
  - **LVC MOS/LVDS X8** (or more): For signals like PPS for time sync.
  - **Display Port:** A display interface for health monitoring/configuring the system.
  - **USB interface X 2(or more):** For supporting HID class for mouse/keyboard interaction.
- **Backplane Connectivity (SpaceVPX):**
  - **Control Plane:** SpaceWire for command, control and configuration.
  - **Utility Plane:** Standard VITA 78 utility signals including 3.3V Aux, 12V power, and I2C/IPMI management.



### 3.2.3 Payload Interface Card / Data Switch

This high-performance computing module is designed to serve as the central payload data aggregation and distribution hub within the SpaceVPX chassis. The Payload Interface Card shall act as a bridge between external high-speed payloads and the internal mass storage array. It shall also be capable to relaying the incoming data to a Processing/Inference card on data plane for AI/ML algorithm compute for the payload data.

*Power Budget= ~60W.*

*Core Responsibilities:*

- **Ingest:** Capture high-speed payload data via multiple Ethernet ports.
- **Process:** Perform formatting and compression on ingested data.
- **Storage Offload:** Transfer data to auxiliary Storage Boards via the Expansion Plane (PCIe Gen 2 or higher) using NVMe or equivalent Protocol.
- **File Management:** Maintain a robust, power-fail-safe RTOS-based file system with strict access controls (Read/Write/Write-Protect).
- **Playback:** Retrieve data from Storage Boards and transmit via an Ethernet port.
- **Computing Offload:** Send payload data to the Processing Card over the Backplane for AI/ML inference or algorithm compute.

*Interfaces:*

- **External:** The system shall support simultaneous data ingest over:
  - **4(or higher) ports x 1000Base-T:** 1G Ethernet (Copper PHY).
  - **3(or higher) ports x 10G-:** 10G Ethernet (Optical PHY).
  - **Display Port:** A suitable display interface shall be implemented for file system display to the onboard Crew.
  - **USB interface X 2(or more):** For supporting HID class for mouse/keyboard interaction to select the files and Mass Storage Class for connection with a portable SSD carried by onboard crew
- **Backplane Connectivity (SpaceVPX):**
  - **Data Plane:** 10GBASE-KR/KX interfaces with other cards.
  - **Control Plane:** SpaceWire for command, control and configurations traffic from the System Controller card.
  - **Expansion Plane:** PCIe Gen 2 (or higher) lanes configured as Root Complex to interface with up to three external Memory Storage cards in **RAID configuration** to support 10Gbps throughput with each memory board.
  - **Utility Plane:** Standard VITA 78 utility signals for I2C/IPMI management.

### 3.2.4 Storage Card

The SpaceVPX (VITA 78) compliant NVMe (or equivalent) based Storage Board shall have a PCIe 2.0 (or higher) interface and provide a storage capacity of 2 TB (or higher, extendable up to 4 TB) based on pseudo single-level cell (SLC) flash storage in a high performance, radiation-tolerant architecture. The Storage board shall support a sustained bandwidth (read and write) of 10 Gbps or higher.

*Power Budget* = ~15W

*Interfaces:*

- **NAND flash devices:** ONFI 4.0 (or higher) compliant NV-DDR3 interface, supporting interface up to 666 MT/s or higher
- **Backplane Connectivity (SpaceVPX):**
  - **Expansion plane:** PCIe Gen 2.0 (or higher)
  - **Control Plane:** SpaceWire for command, control and configurations traffic from the System Controller card.
  - **Utility Plane:** Standard VITA 78 utility signals for I2C/IPMI management.

*Features:*

- The vendor shall implement **Flash Translation Layer (FTL), garbage collection algorithms, Wear Levelling algorithms, Bad Block management etc** as required for NAND Flash Memories.
- **Power Fail Protection:** The board shall include a hold-up circuit (capacitance bank) capable of sustaining operation after power loss to allow the controller to flush volatile data to NAND Flash memories or any other methodology for database retrieval during an abrupt power failure.

### 3.2.5 Processing/Inference Card

The Space Grade Processing/Inference Board shall be a high-performance computing module compliant with SpaceVPX (VITA 78) standard and capable of executing AI/ML inference or reconfigurable Edge-computing algorithms.

*Power Budget* = ~25W

*Interfaces:*

- **Backplane Connectivity (SpaceVPX):**
  - **Data Plane: 3(or higher) ports of 10G** - 10G Ethernet interfaces routed directly via Data Plane.
  - **Control Plane:** SpaceWire for command, control and configurations traffic from the System Controller card.
  - **Utility Plane:** Standard VITA 78 utility signals for I2C/IPMI management.

## 4 Vendor selection

The vendor selection is a process to ensure that only industries with the capability to carryout high-speed digital and mechanical designs are part of the further process.

Prospective vendors must provide documentary proof (Purchase Orders, Completion Certificates, Datasheets, or Design Reports) for the following criteria. A detailed list of the vendor qualification criterion is provided in the table 3 which needs to be provided by all the interested industries. These responses will be evaluated by URSC and those vendors who are able to provide all the data and proofs for meeting all the criterion only will be selected for further process.

Based on EOI received and organization's requirement, URSC committee reserves the right for approval/rejection of any criteria.

Table 3: Vendor qualification Criteria

Sl. No.	Criterion Area	Specific Requirement	Evidence
1	SpaceVPX / High-Speed VPX Backplane Design	Experience in designing SpaceVPX (VITA 78) compliant systems or high-speed VPX backplanes supporting protocols (e.g., 10G Ethernet, PCIe Gen 2.0).	Demonstration/ Design reports of similar hardware.
2	High-Speed Networking (10G Ethernet)	Proven capability in designing boards with 10G Ethernet interfaces and implementing TCP/UDP offload engines in FPGA or SoC.	Demonstration/ Design reports or Test logs showing 10Gbps throughput with BER < $10^{-12}$ for a period of 24 hr.
3	NVMe (or equivalent) Storage & FTL Development	Experience in high capacity high speed (2TB or more, 10 Gbps throughput) NVMe-based (or equivalent) storage solutions.	Demonstration/ Design report/Test logs showing 10Gbps throughput
4	Interfaces capabilities	Capability to interface with Payloads over interfaces like TSN Ethernet/ USB/ RS-422/ RS-232/ SpaceWire/ SPI/ LVDS/ Ser-Deser	Demonstration/ Design report
5	IP core capabilities	Experience in designing with IP cores (hard/soft) related to Ethernet MAC, TCP/UDP offload engine, NVMe controller, memory controllers, High-speed transceivers for implementing PCIe 2.0 (or higher) etc	Demonstration/ Design report



6	Software capabilities	Experience in design and development with softwares at various layers – 1. device driver development for Networking, USB, SPI, SpW etc 2. Working experience with RTOS e.g. VxWorks/Linux supporting file management, NvME stack etc 3. Application software	Demonstration/ Design report
7	RAID for Storage boards	Knowledge/ experience in RAID (Striping + Parity) configuration for Storage boards	Demonstration/Design reports
8	TSN ethernet	Knowledge/ experience in implementation of Time Sensitive Ethernet for payload interfaces.	Demonstration/Design reports
9	Heterogeneous Computing (SoC + FPGA)	Experience in designing complex boards integrating Space-grade or equivalent SoCs with 64-bit processor (e.g., ARM Cortex / RISC-V), operating @ 1.2 Ghz or better and having required peripherals and running with RTOS like Linux/Vxworks etc with High-Performance FPGAs (e.g., Xilinx UltraScale/Versal/Polar Fire SOC) sharing high-bandwidth interconnects.	Demonstration/ Design report of in-house developed boards utilizing similar architectures.
10	AI/ML Hardware Acceleration	Capability to develop Edge-computing platforms and deploy AI/ML inference models (CNNs/RNNs) on the same.	Demonstration/ Design report detailing AI model deployment and performance metrics.
11	MIL-STD-1553	Experience in MIL-STD-1553(RT/MT/BC) designs.	Demonstration/ Design report
12	Data Security	Experience in handling data security protocols like AES-256	Demonstration/ Design report
13	Power supply Electronics	Experience in Isolated DC-DC converters (better than 200W) in SpaceVPX/VPX platform.	Demonstration/ Design report
14	Thermal Management	Expertise in Conduction/ radiation-cooled chassis design for high-power modules (~100W)	Thermal analysis reports of high-power



		per slot) in vacuum environments.	dissipating avionics packages.
15	Signal & Power Integrity Analysis	Capability to perform and validate Signal & Power Integrity Analysis for high speed designs like DDR4 (2400 MT/s), PCIe Gen2/3, and 10G Ethernet.	Signal & Power Integrity Analysis reports for high-speed interfaces.
16	Radiation Hardening & Reliability	Experience/ understanding in Radiation Mitigation techniques (eg. TMR, Scrubbing, EDAC etc).	Design reports
17	Package level testing	Experience in package level testing of Digital systems in a single package/card.	Demonstration/Test report
18	ESD safe lab	Vendor should have an ESD safe laboratory and of minimum space > 100 square meter, which can be inspected.	Supporting documents
19	PCB assembly	Experience in PCB assembly with passives 0402 style, BGA packages etc	Demonstration/report
20	Mechanical package design	Experience in mechanical package design qualified for Aerospace standard.	Demonstration/Design report
21	Structural Analysis	Experience in the following structural analysis <ul style="list-style-type: none"> <li>• Static Analysis</li> <li>• Free Vibration/Modal Analysis</li> <li>• Frequency Response Analysis</li> <li>• Transient Response analysis</li> <li>• Random Vibration Analysis</li> <li>• Shock Response Analysis</li> </ul>	Analysis reports
22	Components sourcing	Experience in sourcing EEE parts from OEM/Authorised Distributors.	Provide POs placed by the vendor on OEM/distributor for the AMD/Micro-semi FPGAs, micro-controller, memories, 1553 related chips



23	EMI-EMC	Organisation should have experience in designing for EMI-EMC specification, conducting EMI-EMC tests and qualifying products as per MIL-STD 461C/E/F/G	EMI/EMC Analysis reports
24	Vibration specification	Organisation should have experience in designing for vibration specification as per Mil-STD-810/DO-160G and conducting vibration tests	Supporting Analysis Reports
25	Tools experience	Experience in working with the following tools: PCB development: Cadence or equivalent Thermal & Structural: Seimens NX tool or equivalent SI/PI: Hyperlynx/ Allegro FPGA: Vivado/Vitis (AMD), Libero SoC (Microsemi) Only Licensed tools to be used for development	Supporting tool reports.
26	Certification support (Desirable)	Experience in certification of hardware and software to DO-254 and DO-178 standards resp.	Supporting certifications
27	Standard Compliance	ISO9001 / AS9100	Valid certificates
28	URSC requires all technical data to be shared by vendor for review and documentation.	Compliance required.	
29	Vendor shall sign a Non-Disclosure agreement with URSC after EOI finalisation.	Compliance required.	



## 5 Format for vendor proposal submission

Vendor shall submit the proposals in the below format:

### 5.1 Company Profile

Table 4: Company Details

Sl No.	Document name	Remarks
1	Organisation structure	
2	Vendor's Project structure	This shall include roles and responsibilities.
3	Vendor Compliance	Compliance for vendor qualification criterion as per table 5
4	Project plan	Shall contain the following <ul style="list-style-type: none"> <li>• Work break down structure</li> <li>• schedule for proto model</li> <li>• Gantt chart &amp; critical path</li> <li>• suggestions to reduce the critical path</li> </ul>
5	List of organisations	Details of organisations/companies who will be collaborating or vendor will be sub-contracting to, for various activities. Vendor should be responsible for final project and product outcome.

### 5.2 Compliance Matrix

Vendor selection is based on the compliance matrix.

Table 5: Compliance Matrix

Sl. No.	Criterion Area	Specific Requirement	Evidence	Compliance (yes/no)	Reference documents (mandatory)
1	SpaceVPX / High-Speed VPX Backplane Design	Experience in designing SpaceVPX (VITA 78) compliant systems or high-speed VPX backplanes supporting protocols (e.g., 10G Ethernet, PCIe Gen 2.0).	Demonstration/ Design reports of similar hardware.		
2	High-Speed Networking (10G Ethernet)	Proven capability in designing boards with 10G Ethernet interfaces and implementing TCP/UDP of-fload engines in FPGA or SoC.	Demonstration/ Design reports or Test logs showing 10Gbps throughput with BER < $10^{-12}$ for a		



			period of 24 hr.		
3	NVMe Storage(or equivalent) & FTL Development	Experience in high capacity high speed (2TB or more, 10 Gbps throughput) NVMe-based (or equivalent) storage solutions.	Demonstration/ Design report/Test logs showing 10Gbps throughput		
4	Interfaces capabilities	Capability to interface with Payloads over interfaces like TSN Ethernet/ USB/ RS-422/ RS-232/ SpaceWire/ SPI/ LVDS/ Ser-Deser	Demonstration/ Design report		
5	IP core capabilities	Experience in designing with IP cores (hard/soft) related to Ethernet MAC, TCP/UDP offload engine, NVMe controller, memory controllers, High-speed transceivers for implementing PCIe 2.0 (or higher) etc	Demonstration/ Design report		
6	Software capabilities	Experience in design and development with softwares at various layers – 1. device driver development for Networking, USB, SPI, SpW etc 2. Working experience with RTOS e.g. VxWorks/Linux supporting file management, NvME stack etc 3. Application software	Demonstration/ Design report		
7	RAID for Storage boards	Knowledge/ experience in RAID (Striping + Parity) configuration for Storage boards	Demonstration/Design reports		
8	TSN ethernet	Knowledge/ experience in implementation of Time Sensitive Ethernet for payload interfaces.	Demonstration/Design reports		
9	Heterogeneous Computing (SoC + FPGA)	Experience in designing complex boards integrating Space-grade or equivalent SoCs with 64-bit processor (e.g., ARM Cortex / RiSCV), operating @ 1.2 Ghz or better and having required peripherals and running with RTOS like Linux/Vxworks etc with High-Performance FPGAs (e.g., Xilinx UltraScale/Versal/Polar Fire SOC) sharing high-bandwidth interconnects.	Demonstration/ Design report of in-house developed boards utilizing similar architectures.		



10	AI/ML Hardware Acceleration	Capability to develop Edge-computing platforms and deploy AI/ML inference models (CNNs/RNNs) on the same.	Demonstration/ Design report detailing AI model deployment and performance metrics.		
11	MIL-STD-1553	Experience in MIL-STD-1553(RT/MT/BC) designs.	Demonstration/ Design report		
12	Data Security	Experience in handling data security protocols like AES-256	Demonstration/ Design report		
13	Power supply Electronics	Experience in Isolated DC-DC converters (better than 200W) in SpaceVPX/VPX platform.	Demonstration/ Design report		
14	Thermal Management	Expertise in Conduction/ radiation-cooled chassis design for high-power modules (~ 100W per slot) in vacuum environments.	Thermal analysis reports of high-power dissipating avionics packages.		
15	Signal & Power Integrity Analysis	Capability to perform and validate Signal & Power Integrity Analysis for high speed designs like DDR4 (2400 MT/s), PCIe Gen2/3, and 10G Ethernet.	Signal & Power Integrity Analysis reports for high-speed interfaces.		
16	Radiation Hardening & Reliability	Experience/ understanding in Radiation Mitigation techniques (e.g. TMR, Scrubbing, EDAC etc).	Design reports		
17	Package level testing	Experience in package level testing of Digital systems in a single package/card.	Demonstration/Test report		
18	ESD safe lab	Vendor should have an ESD safe laboratory and of minimum space > 100 square meter, which can be inspected.	Supporting documents		
19	PCB assembly	Experience in PCB assembly with passives 0402 style, BGA packages etc	Demonstration/report		



20	Mechanical package design	Experience in mechanical package design qualified for Aerospace standard.	Demonstration/Design report		
21	Structural Analysis	Experience in the following structural analysis <ul style="list-style-type: none"> <li>• Static Analysis</li> <li>• Free Vibration/Modal Analysis</li> <li>• Frequency Response Analysis</li> <li>• Transient Response analysis</li> <li>• Random Vibration Analysis</li> <li>• Shock Response Analysis</li> </ul>	Analysis reports		
22	Components sourcing	Experience in sourcing EEE parts from OEM/Authorised Distributors.	Provide POs placed by the vendor on OEM/distributor for the AMD/Microsemi FPGAs, microcontroller, memories, 1553 related chips		
23	EMI-EMC	Organisation should have experience in designing for EMI-EMC specification, conducting EMI-EMC tests and qualifying products as per MIL-STD 461C/E/F/G	EMI/EMC Analysis reports		
24	Vibration specification	Organisation should have experience in designing for vibration specification as per Mil-STD-810/DO-160G and conducting vibration tests	Supporting Analysis Reports		
25	Tools experience	Experience in working with the following tools: PCB development: Cadence or equivalent Thermal & Structural: Seimens NX tool or equivalent SI/PI: Hyperlynx/ Allegro	Supporting tool reports.		



		FPGA: Vivado/Vitis (AMD), Libero SoC (Microsemi) Only Licensed tools to be used for development			
26	Certification support (Desirable)	Experience in certification of hardware and software to DO-254 and DO-178 standards resp.	Supporting certifications		
27	Standard Compliance	ISO9001 / AS9100	Valid certificates		
28	URSC requires all technical data to be shared by vendor for review and documentation.	Compliance required.			
29	Vendor shall sign a Non-Disclosure agreement with URSC after EOI finalization	Compliance required.			

### 5.3 Annexures/References

Supporting documents to be put as part of this section.