भारत सरकार / **Government of India**
अंतरिक्ष विभाग / **Department of Space**
यू.आर. राव उपग्रह केंद्र / **U.R.RAO SATELLITE CENTRE**
एच.ए.एल. एयरपोर्ट रोड, विमानापुरा डाक / **HAL Airport Road, Vimanapura Post,**
बेंगलूरु/ **BENGALURU – 560 017**

संदर्भ संख्या/Ref No.:**URSC/PUR/ISDC2025-0-64003/EoI/2025-26** **12.06.2025**

एकीकृत एवियोनिक्स पैकेज (IAP) के लिए परीक्षण प्रणाली के कार्यान्वयन तथा परियोजना गतिविधियों के दौरान परीक्षण प्रणाली गतिविधियों को सहायता प्रदान करने के लिए इच्छा की अभिव्यक्ति [EoI] के लिए आमंत्रण।

Invitation for Expression of Interest [EoI] for Realisation of the test system for Integrated Avionics Packages (IAP) and provide support to the test system activities during project activities.

भारत सरकार के अंतरिक्ष विभाग के अंतर्गत भारतीय अंतरिक्ष अनुसंधान संगठन इसरो का यू आर राव उपग्रह केंद्र [यू आर एस सी] (जिसे पहले इसरो उपग्रह केंद्र के नाम से जाना जाता था), सभी भारतीय निर्मित उपग्रहों के डिजाइन, विकास, निर्माण तथा परीक्षण के लिए जिम्मेदार है। यू आर एस सी वर्तमान में एकीकृत एवियोनिक्स पैकेज (आई ए पी) के लिए परीक्षण प्रणाली के कार्यान्वयन तथा परियोजना गतिविधियों के दौरान परीक्षण प्रणाली गतिविधियों को सहायता प्रदान करने के लिए उद्योग भागीदारों को आमंत्रित कर रहा है।

U.R. Rao Satellite Centre [URSC] (Formerly known as ISRO Satellite Centre), of Indian Space Research Organization [ISRO] under Department of Space, Government of India is responsible for Design, Development, Fabrication and Testing of all Indian made Satellites. URSC is currently inviting Industry Partners to carry out the **realisation of the test system for Integrated Avionics Packages (IAP) and provide support to the test system activities during project activities.**

यू आर एस सी उद्योग को आईएपी के लिए परीक्षण प्रणाली के आद्यांत से अंतिम विकास को स्वतंत्र रूप से करने में सक्षम बनाने तथा अंतरिक्ष यान से संबंधित गतिविधियों को करने के लिए निजी अंतरिक्ष उद्योगों में कुशल जनशक्ति विकसित करने के लिए स्थापना/रखरखाव और संचालन सहायता प्रदान करने में रुचि रखता है।

URSC is interested to enable the industry to carry out independently the end-to-end development of test system for IAP and provide the installation/maintenance and operation support to develop skilled manpower in the private space industries to carry out spacecraft related activities.

केवल उन भारतीय उद्योगों से इच्छा की अभिव्यक्ति को आमंत्रित करने का प्रस्ताव है जिनके पास आईएपी के लिए परीक्षण प्रणाली के डिजाइन, विकास और कार्यान्वयन को निष्पादित करने तथा परियोजना गतिविधियों के दौरान परीक्षण प्रणाली गतिविधियों को सहायता प्रदान करने के लिए तकनीकी अवसंरचना और क्षमता है।

The proposal is to invite Expression of Interest exclusively from Indian industries having technical infrastructure and capability to execute **design, development and realisation of test system for IAP and support to the test system activities during project activities**

ई ओ आई दस्तावेज हमारे वेबसाइट www.isro.gov.in से डाउनलोड किए जा सकते हैं
EOI documents can be downloaded from our website www.isro.gov.in

ई ओ आई का मूल्यांकन बोलीदाताओं के अनुभव, सेवाओं के दायरे की उनकी समझ, सुविधा अवसंरचना, प्रस्तावित कार्यप्रणाली और कार्य योजना, कुशल जनशक्ति और उद्योग की वित्तीय ताकत के आधार पर किया जाएगा।
The EOI will be evaluated on the basis of bidder's experience, its understanding of scope of services, facility infrastructure, proposed methodology and work plan, skilled manpower and the financial strength of the industry.

यूआरएससी आवश्यकता पड़ने पर ईओआई की प्रक्रिया को रद्द/पुनः जारी करने या आगे की जानकारी/विवरण मांगने का अधिकार सुरक्षित रखता है।
URSC reserves the right to cancel/re-issue the process of EOI if the necessity so arises or to seek further information/details.

यदि कोई कंपनी/फर्म किसी भ्रष्ट या धोखाधड़ीपूर्ण व्यवहार में लिप्त पाई जाती है, तो उसे निविदा प्रक्रिया में भाग लेने से रोक दिया जाएगा और उसके ईओआई दस्तावेज़ पर विचार नहीं किया जाएगा।
Companies/Firms, if found to have indulged in any corrupt or fraudulent practices, will be debarred taking part in the Tendering process and their EOI Document will not be taken up for consideration.

इच्छा की अभिव्यक्ति के साथ-साथ आपूर्तिकर्ताओं/फर्मों को निम्नलिखित जानकारी भी विस्तार से प्रस्तुत करनी चाहिए:
Along with "Expression of Interest" Suppliers/ Firm[s]should furnish the following information also in detail:

1. कंपनियों का पंजीकृत पता के साथ, फोन, फैक्स, ईमेल, वेब आदि।
   Registered address of the Companies with Phone, Fax, Email, Web etc.
2. कंपनी/संगठन की स्थिति (स्वामित्व/साझेदारी/निजी/सार्वजनिक लिमिटेड आदि) के साथ मालिक, भागीदारों, निदेशक मंडल आदि के नाम और पता।
   Company/Organization Status (Proprietary/Partnership/Private/Public Ltd. etc.) with Name and Address of Proprietor, Partners, Board of Directors, etc.
3. सहयोगी: (ए) भारतीय (बी) विदेशी।
   Associates: (a) Indian (b) Foreign.
4. पि□ ले 3 वर्षों के दौरान प्रमुख ग्राहकों की सूची, पूर्ण पता और उनके संपर्क व्यक्ति।
   List of Major Customers during the last 3 Years with full address and their Contact Persons.
5. स्वामित्व वाली/उपलब्ध अवसंरचना सुविधाओं का विवरण।
   Details of Infrastructure Facilities owned / available.
6. कंपनी के प्रमुख शेयरधारकों के नाम और पते तथा उनकी शेयर पूंजी का प्रतिशत।
   Names and addresses of the major Shareholders of the Company and the percentage of their share capital.
7. नवीनतम वार्षिक रिपोर्ट की प्रति के साथ पि□ ले 3 वित्तीय वर्षों के लिए पूंजी और कारोबार।
   Capital and Turnover for the preceding 3 Financial Years with copy of latest Annual Report.
8. उपलब्ध/वित्तीय क्षमता क्रेडिड सुविधाएं।
   Financial Capacity/Credit facilities available.
9. बैंकरों का नाम और पता।
   Name and Address of Bankers.
10. व्यापार संघ जिससे उद्योग/उद्योग जुड़े हुए हैं।
    Trade Association to which Industry/ies belong to.

11. संस्था/बिक्री/सेवा कर पंजीकरण संख्या।
    Establishment/Sales/Service Tax Registration Number.
12. व्यापार का प्रकार।
    Nature of Business
13. उनके बैंकरों द्वारा जारी फर्म की सॉल्वेंसी/वित्तीय क्षमता।
    Solvency/Financial capacity of the Firm issued by their Bankers.
14. उद्योगों की अन्य कोई प्रासंगिक जानकारियाँ हैं।
    Any other information the Industry/ies consider relevant.
15. सामर्थ्य और कमियों के क्षेत्रों को स्पष्टतः प्रकट करते हुए कंपनी/कंपनियों के प्रोफाइल
    The Profile of the Company/ies clearly bringing out the areas of Strength and Weaknesses.
16. ई ओ आई में भाग लेने के लिए तकनीकी और संगठनात्मक सामर्थ्य का स्व-मूल्यांकन।
    Self-Assessment Technical and Organizational Competence to take part in the EOI.
17. ई ओ आई में उल्लिखित प्रत्युत्तर प्रपत्र
    Response forms as mentioned in the EoI

<u>ईओआई प्रतिक्रिया को पूरा करना/**Completion of the EOI Response:**</u>

a. कंपनी/फर्म को ईओआई दस्तावेजों में सभी निर्देशों, नियमों और शर्तों, प्रपत्रों, आवश्यकताओं और अन्य सूचनाओं का सावधानीपूर्वक अध्ययन करने की सलाह दी जाती है। ईओआई प्रस्तुत करना ईओआई दस्तावेजों के सावधानीपूर्वक अध्ययन और जांच के बाद किया गया माना जाएगा, जिसमें इसके निहितार्थों की पूरी समझ हो।
   The Company/Firms are advised to study all the instructions; Terms and Conditions; Forms; Requirements and other information in the EOI documents carefully. The submission of EOI shall be deemed to have been done after a careful study and examination of the EOI documents with full understanding of its implications.

b. इस ई ओ आई का जवाब सभी मामलों में पूर्ण और संपूर्ण होना चाहिए। ई ओ आई दस्तावेज द्वारा आवश्यक सभी जानकारी प्रस्तुत करने में विफलता या ईओआई दस्तावेजों के हर पहलू के प्रति पर्याप्त रूप से उत्तरदायी न होने वाला प्रस्ताव प्रस्तुत करना कंपनी/फर्म के जोखिम पर होगा और इसके परिणामस्वरूप दस्तावेज को अस्वीकार किया जा सकता है।
   The response to this EOI should be full and complete in all respect. Failure to furnish all the information required by the EOI document or submission of proposal not substantially responsive to the EOI documents to every aspect will be at the risk of the Company/Firms and may result in rejection of the document.

c. प्रस्तुत किए गए ईओआई के सभी पृष्ठों पर क्रमांक होना चाहिए और अधिकृत हस्ताक्षरकर्ता द्वारा हस्ताक्षरित होना चाहिए।
   All the pages of the EOI submitted must be numbered and signed by the authorized signatory.

d. ई ओ आई के संबंध में प्रचार करना सख्त वर्जित है और एजेंसी द्वारा प्रस्तुत किए गए ऐसे प्रचार किए गए ईओआई को अस्वीकार किया जा सकता है।
   Canvassing in connection with the EOI be strictly prohibited and such canvassed EOI submitted by the Agency are liable to be rejected.

उपरोक्त सभी जानकारी के साथ इच्छा की अभिव्यक्ति नीचे दिए गए पते पर, उपरोक्त संदर्भ संख्या का उल्लेख करते हुए, नियत तिथि और समय तक पहुंच जानी चाहिए।
"Expression of Interest" with all the above information shall reach the address given below, quoting the above Reference Number on or before the due date & time.

वरिष्ठ प्रमुख, क्रय एवं भंडार/Sr. Head, Purchase & Stores
यू आर राव उपग्रह केंद्र/U R Rao Satellite Centre,
एचएएल एयरपोर्ट रोड/HAL Airport Road,
Vimanapura Post, Bengaluru/विमानपुरा पोस्ट, बेंगलुरु 560 017,
कर्नाटक, भारत/Karnataka, India

कृपया ईओआई संख्या का उल्लेख करते हुए अपने स्पष्टीकरण ई-मेल पर भेजें: pso_e@ursc.gov.in. ईओआई से संबधित सभी स्पष्टीकरण का उत्तर प्री-ईओआई मीटिंग में दिया जाएगा। प्री-ईओआई मीटिंग में भाग लेने के लिए अनुरोध 25.06.2025 14:00 IST को या उससे पहले यहाँ उल्लिखित ई-मेल पर पहुँच जाना चाहिए। हालाँकि, ईओआई (हार्डकॉपी) का जवाब केवल ऊपर उल्लिखित डाक पते पर भेजा जाएगा)। ईमेल और फैक्स कोटेशन स्वीकार्य नहीं हैं। नियत तिथि और समय के बाद प्राप्त कोटेशन स्वीकार्य नहीं हैं।
Please address your clarifications quoting the EOI number to E-mail: pso_e@ursc.gov.in. All queries related to EOI will be addressed in the Pre-EOI meeting. Request for participation in Pre-EoI meeting shall reach on or before 25.06.2025 14:00IST to the Email mentioned herein. However, response to EOI (hardcopy) shall be sent to above mentioned postal address only. **E-mail & Fax quotations are not acceptable. Quotation received after due date & time are not acceptable.**

स्पष्टीकरण प्रस्तुत करने की अंतिम तिथि Last date of submission of clarification	:	24.06.2025 10:00 Hrs IST.
प्री-ईओआई बैठक (,सम्मेलन कक्ष, स्वगत कक्ष, यू आर एस सी में): Pre-EOI meeting (at Conference Hall, Reception, URSC)	:	26.06.2025 13:30 Hrs IST.
ईओआई प्रस्तुत करने की अंतिम तिथि Last date for submission of EOI	:	**17.07.2025 13:00 Hrs IST.**
ई ओ आई की खुलने की तिथि Opening date of EOI	:	**17.07.2025 14:00 Hrs IST.**

उपरोक्त सभी जानकारी के साथ इच्छा की अभिव्यक्ति 17.07.2025 13:00 IST बजे तक या उससे पहले उपरोक्त संदर्भ संख्या का उल्लेख करते हुए, नीचे हस्ताक्षरकर्ता तक पहुँच जानी चाहिए। यह प्रस्ताव पूर्व-ईओआई योग्यता के रूप में आरंभ किया गया है। यूआरएससी बिना कोई कारण बताए सभी या किसी भी इच्छा की अभिव्यक्ति को स्वीकार या अस्वीकार करने का अधिकार सुरक्षित रखता है।
“Expression of Interest” with all the above information shall reach the undersigned, Quoting above Reference Number on or before **17.07.2025 13:00 IST**. This proposal is initiated as a Pre-EOI Qualification. URSC reserves the right to accept or reject all or any such “Expression of Interest” without assigning any reasons what so ever.

[Sd]

वरिष्ठ प्रधान, क्रय एवं भंडार
Sr. Head, Purchase & Stores

EOI proposal for IAP test system

Task team for IAP test system realisation

U R Rao satellite Centre

Bangalore-560017

Contents

1 Introduction:

URSC is developing an integrated Avionics Package, which integrates the On-Board Computer (OBC), Baseband Data Handling (BDH), Solid State Recorder (SSR), Satellite Positioning System (SPS), Telemetry and Tele command System (TTC) and Payload data transmitter RF chain functions into a single package with a goal to meet less volume, weight and power consumption for various satellite platforms.

To test and evaluate this avionics hardware, a specialized test system to simulate the various interfaces of the spacecraft is a necessity. This document brings out the requirements for a modular test system for the test and evaluation of Integrated Avionics Package Hardware for spacecraft bus upto I1K class with intent to develop the product through industry.

Proposals are invited by industries for the realisation of the test system and provide support to the test system activities during project activities.

2 Scope of the Work

The scope of the work involves the development, integration and end to end test of testing of test system for the complete test and evaluation of the integrated avionics package in different configurations. Mainly with two configurations; one with OBC+ SPS+ Data handling &Storage + RF and other excluding OBC ie SPS+ Data handling &Storage + RF. Test system proposed should cater for both the configuration with required interface simulations.

The proposal involves the following broad level activities:

2.1 Test system Design, realisation and Evaluation

Under this activity vendor is expected to configure the test system according to specifications, design, complete the reviews and realise the test system hardware and required software and demonstrate the test system for the functionalities.

2.2 Test system configuration for Identified Project

Under this activity vendor is expected to complete the configuration of the Test system for UUT for the identified project with required wiring which includes harness requirements for the Project, stimuli and interface configurations and databases and complete the test and evaluation of the test system for connecting to onboard packages.

2.3 Test system support activities for Project T& E activities

Under this activity vendor is expected to provide the support for setting up the test system at various test requirements like T&E, Vibration lab, EMI/EMC lab, Thermovac facilities, to complete evaluation, and maintain the test system to complete the activities of T&E of system under test.

3 Test System design:

The Test System shall simulate all the electrical signals of IAP which includes different interfaces like discrete, serial, Mil-std-1553B, LVDS, SerDes, MGT, optical interface, Serial

interfaces like SPI, RS485, Ethernet, USB, I2C etc. Detailed specifications are provided in the respective sections. The test system unit needs to be controlled by software to feed the required signals to the Unit under test (UUT).

The driver software has to be in Linux as per the requirement and specifications mentioned. API (application program interface) or software library needs to be supplied along with the unit for building the application software. The test system also involves the harness to connect the UUT to test system. Harness needs to be validated for both connection and cross connection.

The test system development involves the procurement; testing and integration of standard instruments, design, testing and integration of URSC specified custom made instrumentation and also end to end design of specified designs. It also involves software design, harness fabrication and Installation/Testing/Maintenance and operation support for the test system.

3.1 The test system major blocks.

Test system consists of following four major blocks.

3.1.1 OBC interface simulation block

3.1.2 SPS interface simulation block

3.1.3 Data handling and storage interface simulation block

3.1.4 RF interface simulation block

The OBC simulator & data logger can be a common block to simulate OBC signals in order to test SPS/Data handling and storage/ RF system independent of OBC during debugging phase.

The overall block diagram is provided in figure1.

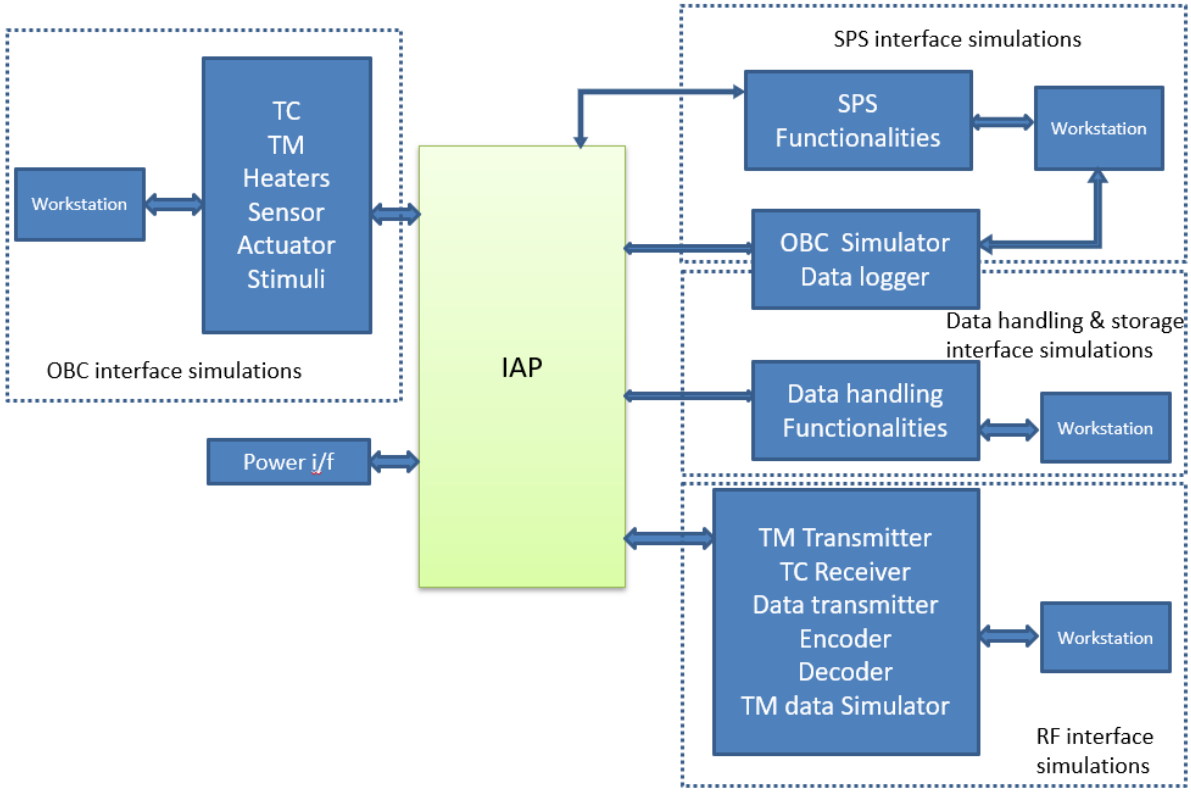


Figure 1: Block diagram of test system

3.2 Building blocks:

Following are the building blocks of test system.

3.2.1 Computer Host system: This is a Linux based computer work station running the main test system application software accessed by User. It also runs UI application. All the four major functions (OBC/SPS/Data handling and storage/RF) will have individual workstation.

3.2.2 Front End Processor: The Front-end processor (FEP) is an industrial PC housing multiple PCI/PCIe/PXIe boards for performing communication with the onboard systems for supporting SPI, RS485, MIL-STD-1553 bus communication, LVDS, CMOS, SERDES, MGT, optical and digital/analog simulations.

3.2.3 10G Ethernet switch/router to connect all the test system equipment

3.2.4 Harness for test system interconnection

3.2.5 Standard PCI/PCIe/PXIe boards to simulate various interfaces like Mil-std-1553B, Analog channels.

3.2.6 Customised Boards to simulate SPI, I2C, RS485 etc as per URSC design

3.2.7 Customised Boards as per the URSC specific requirements wherein requirements will be provided and vendor has to design and realise the boards

3.2.8 Customised Boards to simulate CMOS, LVDS, SERDES 217, TLK 2711, MGT, Optical as per URSC specific requirements.

3.2.9 Customized board for temperature, analog voltage, opto-coupler interface, current monitoring, 5V/28V pulse commands with programmable width and digital IOs with logging feature.

3.2.10 Standard instruments like TTCP (ex: cortex TTCP), HSDR and GNSS Record & replay/Simulator

3.2.11 Standard Instrumentation& Units common to all functions

3.2.11.1 Current Meters & Power Supplies

3.2.11.2 Digital table top Multimeters

3.2.11.3 Digital Storage Oscilloscope– upto 2.5GHz

3.2.11.4 Waveform generator

3.2.11.5 Spectrum Analyzer

3.2.11.6 Frequency counter

3.2.11.7 Rack Enclosures

3.2.12 Software Requirements:

3.2.12.1 Front End Processor software (URSC designed)/ (vendor designed)

3.2.12.2 Host Software with GUI (URSC designed)/(vendor designed)

3.2.12.3 Device Driver software (Available with URSC for standard specified modules)

3.2.12.4 FEP software (Customised by Vendor – if hardware design is modified)

3.2.12.5 Device Driver software (Vendor- If customised hardware is proposed)

3.2.12.6 Test system designed should enable test automation.

3.2.12.7 Software source codes, library files required for commanding/configuring the test system and UUT, data acquisition, data processing and debugging to be provided.

4 Test system Functional description

4.1 Functional description for the test requirements of OBC functionalities:

4.1.1 OBC functionalities Introduction:

The OBC functionalities of the Integrated Avionics Hardware of a spacecraft includes the interfaces with communication systems for Telemetry and Telecommand Data flow, command distribution and telemetry acquisition through discrete and bus interfaces, sensor and actuator interfaces for the attitude and orbital control. It carries out various functions (hardware and software) to exercise these interfaces for various scenarios of operation. To test and evaluate the avionics hardware, a specialized test system to emulate the various interfaces of the spacecraft is a necessity.

4.1.2 Overview:

Block diagram of a generic test system used for the complete evaluation of OBC functionalities is shown in Figure 2. The IAP is connected to the test system through a bulk harness typically supporting few thousand interconnections. Industrial PC, Current meters, power supplies, Test Interface Package, Heater & Thruster Load unit, Sensor Stimuli Unit and Interface Units are integrated into a 19-inch industrial rack system and is controlled by a host workstation remotely.

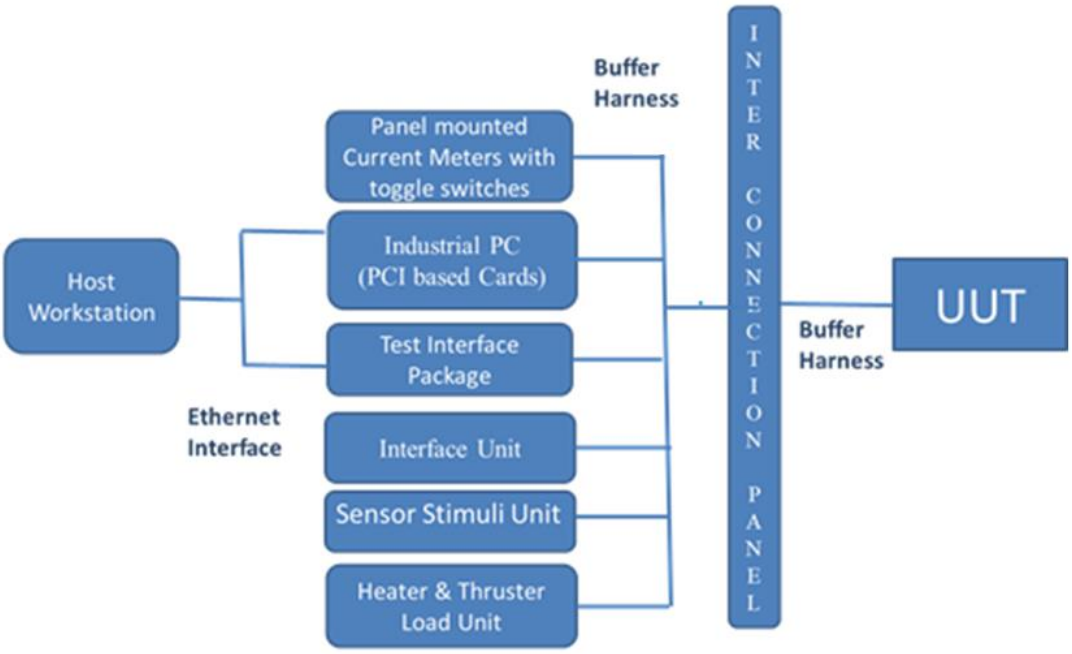


Figure 2: Test requirements to test OBC functionalities

Following are the specific customised units for the testing of OBC functionalities. For all these units, design will be provided by URSC.

4.1.3 Test Interface package: It is a hardware unit of the test system to sense and measure electrical and timing values of the various command outputs coming from avionics hardware. The measurement data is transferred to Host through Ethernet interface

4.1.4 Sensor Stimuli Unit& Interface unit: This unit generates the stimuli to imitate the different sensors interfaced with the onboard package in the form of resistance, voltage and current. The stimuli are controlled by host.

4.1.5 Heater & Thruster Load Unit: Load unit contains high wattage loads required to simulate the heater and actuator loads of a spacecraft for testing the corresponding onboard hardware interfaces

4.1.6 PC Add on cards:

4.1.6.1 PCI based DAC card

4.1.6.2 PCI Based Mil-std-1553 BC, Multi RT& MT simulator

4.1.6.3 PCI based SPI and RS485 interface card

4.1.6.4 Xilinx based Digital I/O Hardware Simulation card -URSC design

All the units of the test system except the host computer are mounted in a 19-inch industrial rack and are interconnected to work as a single unit.

4.2 Functional description for the test requirements of SPS functionalities:

4.2.1 Introduction to test requirements of SPS functionalities

A GNSS signal source, measuring/calibrating instruments, clock source, multimeter and digital oscilloscopes and OBC interface simulators are required for testing and evaluation of SPS at standalone or integrated level. The typical test setup for SPS is shown in the figure below:

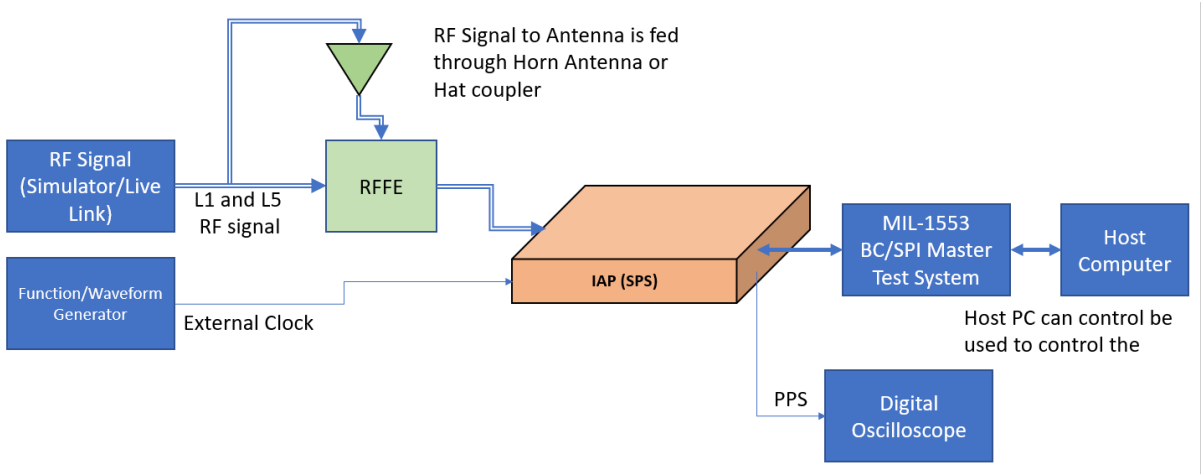


Figure3: SPS Functionality test setup

4.2.2 Basic functional requirements

4.2.2.1 GNSS signal source

The RF source to test and evaluate the performance of SPS can be a GNSS Simulator or GNSS record and replay or a Vector Signal Generator witha GNSS Simulator feature.

4.2.2.2 OBC interface simulator

FPGA based PCI board housed in an Industrial PC (FEP) which supports multiple communication protocols (I2C, SPI, MIL-STD-1553B) and voltage levels (5V and 3.3V) for command generation and reception, thermistor reading and logging, analog (-5V to +5V) monitoring and logging. Involves both FPGA design and software design to build the applications of bus controller, bus monitor and data processing & extraction for Mil-std-1553B bus.

4.2.2.3 Clock Source:

A Temperature Controlled Crystal Oscillator (TCXO) or external clock to calibrate the Pulse Per Second (PPS) with an accuracy of ±50ns.

4.2.2.4 SPS HOST COMPUTER GUI Software:

It receives data from the FEP displays it in a user-friendly interface on the HOST COMPUTER. Provides tools for data analysis, visualization, logging, verification and archival of the data for further processing. This will be a vendor designed software.

4.2.2.5 Voltage Level Shifter:

Board to ensure compatibility between the Test System and the SPS by converting voltage levels (5V and 3.3V levels) single ended voltage levels (CMOS 5V and LVCMOS 3.3V) for command generation and single ended voltage levels (CMOS 5V and LVCMOS 3.3V) /differential (LVDS 2.5/3.3V) reception.

4.3 Functional description for the test requirements of RF functionalities:

4.3.1 Introduction to RF functionalities:

The RF system is required to cater to the functions of tele-command reception and telemetry and payload data transmission.

4.3.1.1 S/X-Band TC Receiver: Receives the RF input signal and performs digitization, acquisition and tracking, TC demodulation, bit synchronization and lock detection of the input signal. Provides TC data, TC clock and lock indication to the TC decoder. It interfaces with RF front end of the receiver. Based on the mission requirement following demodulation schemes shall be used.

- Sub-carrier based (PCM/PSK/PM, PCM/PSK/FM etc.)
- Direct modulation (DSSS-BPSK, DSSS-UQPSK, direct BPSK, QPSK etc.)
- Tone and regenerative PN Ranging

4.3.1.2 S/X-Band TM Transmitter: It performs modulation of the TM data and interfaces with the RF power amplifiers of the transmitter. Based on the mission requirement following modulation schemes shall be used.

- BPSK/CDMA/PSK-PM basedTelemetry transmission
- Tone and regenerative PN ranging
- The block diagram is provided in figure 4.

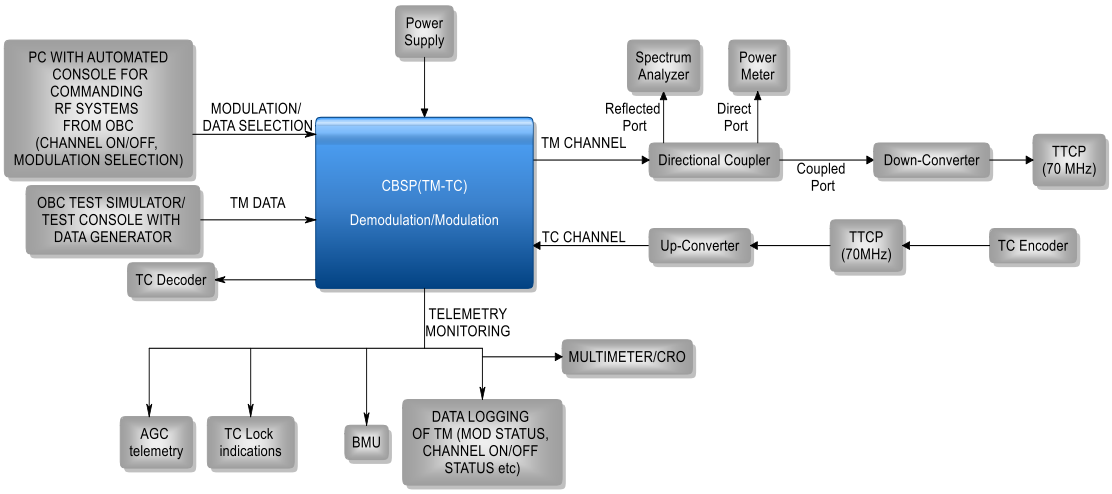


Figure 4: TT&C test system block diagram

4.3.1.3 X-Band Data Transmitter: It is used to transmit the payload data of satellite to the ground station. The modulation scheme is reconfigurable such as BPSK/QPSK/OQPSK/8-PSK/FACM etc and can be changed on demand. Depending on the mission requirements, modulation scheme will be decided.

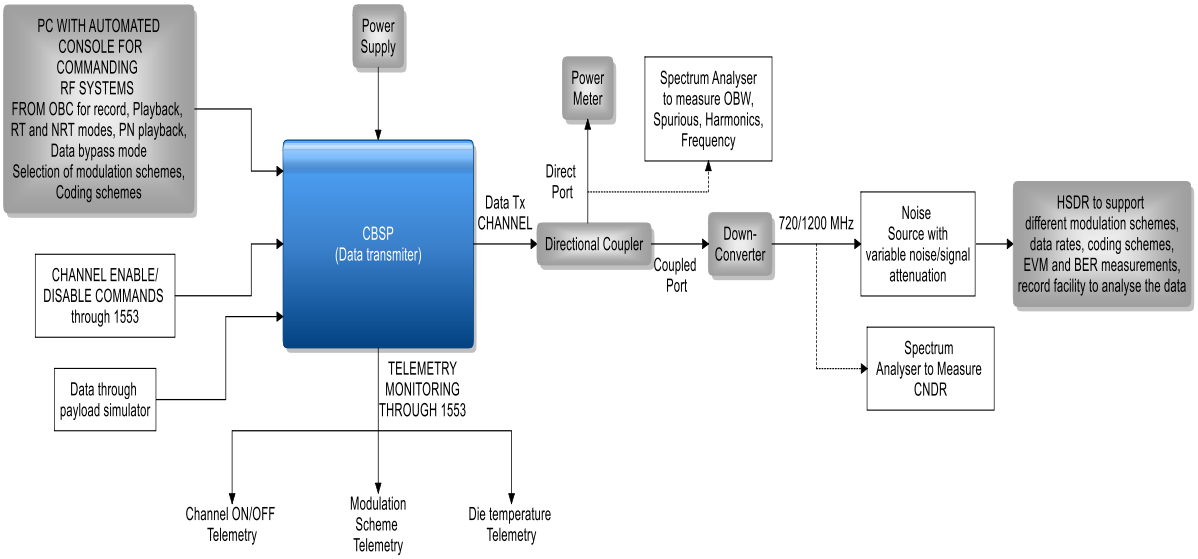


Figure 5: X-band test system block diagram

Test Setup has to evaluate these functionalities and has to ensure, the RF systems meets the specifications required by the mission.

4.3.2 Basic functional requirements

4.3.2.1 TM data simulator/ TC data simulator:

PC based card that simulates TC/ TM data and payload data in different formats / coding required by the package. It also includes encoder and decoder for TC data.

4.3.2.2 TTCP:

Two types of TTCPs are required.

1. TTCP: for S band TTCP with support for tone and PN ranging.
2. HSDR (4G+ supporting FACM): for X band

4.3.2.3 Down converters and Up converters:

For conversion of 70 MHz signal to/from S/X-band RF signal

4.3.2.4 Noise generator:

For threshold measurement

4.3.2.5 Spectrum Analyser

For measurement of RF spectrum at L/S/X-Band.

4.3.2.6 Power Meter

For measurement of RF power at S/X-Band.

4.3.2.7 RF Cables and Adaptors

Cables and adapters required for interconnections between UUT and equipment

- RF attenuators to test the dynamic range of receiver.

4.3.2.8 Directional Coupler

It is required for splitting RF signal and distributing it to multiple equipment for simultaneous monitoring.

4.3.2.9 Frequency Counter

- Frequency Range: upto 12 GHz

4.4 Functional description for the test requirements of Data handling functionalities:

Data Handling systems acquires the data from payloads/sensors as well as auxiliary data from Master Computer, format the same, transmit the data with channel coding in real time based on the spacecraft visibility to ground or store the data in solid state recorder and playback the same during ground visibility to the spacecraft. The functions which needs to be validated are very critical to the mission operations such as DC-DC and Controller logic, Payload interface logic, Record/Real time Formatting Logic, Downlink Formatting Logic and FDIRs. To test these functionalities test systems are also required along with software development.

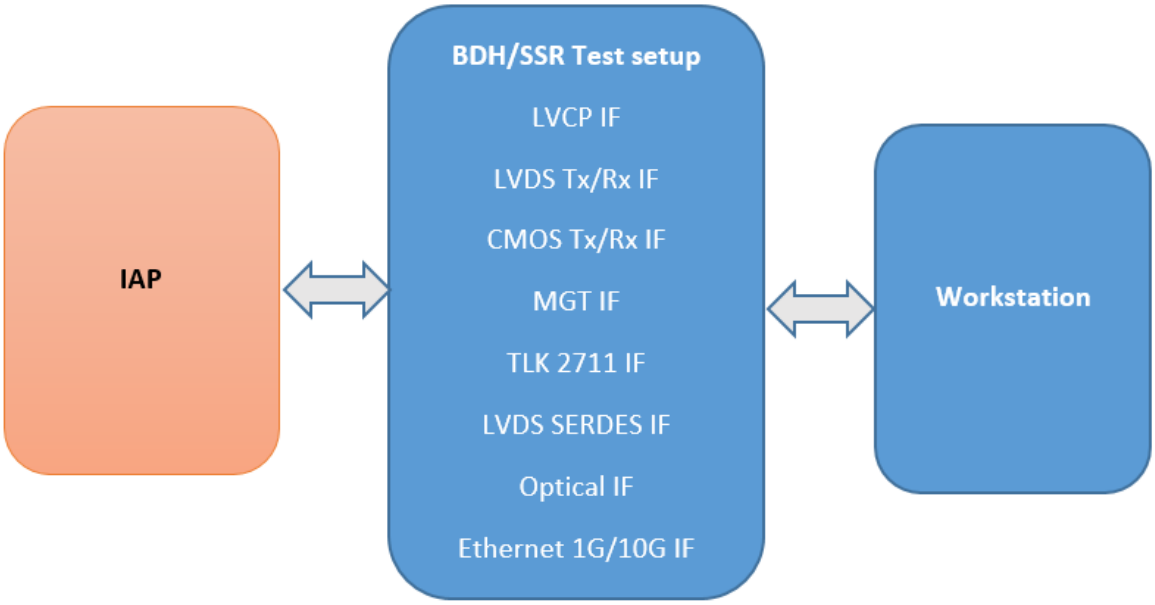


Figure 6: BDH/SSR test system block diagram

4.4.1 Basic functional requirements

Following are the basic functional blocks required in the test system. It should simulate the payload data in different interface formats and data rates. The above feature/functions have to be realized in standard chassis (Backplane/daughter board configuration). Per daughter board data rate handling capacity shall be 8Gbps or better. Accordingly, backplane shall be able to handle total throughput required to meet the system specification. This system will be connected to a host workstation, wherein user interface for auto testing/ logging and archival of data to be done.

4.4.1.1 LVDS interface simulators:

Payload Data simulation with LVDS transmitters and Data acquisition through LVDS receivers.

4.4.1.2 LVCP interface simulators:

Payload Data simulation with LVCP transmitters and Data acquisition through LVCP receivers

4.4.1.3 MGT interface

Payload Data/Ethernet data simulation with MGT transmitters and payload Data/Ethernet data acquisition with MGT receivers.

4.4.1.4 CMOS interface

Payload Data simulation with CMOS transmitters and data acquisition through receivers.

4.4.1.5 TLK2711

Payload Data simulation with TLK2711 transmitters and Payload Data acquisition with TLK2711 receivers.

4.4.1.6 LVDS SERDES

Payload Data simulation with LVDS217 transmitters and Payload Data acquisition with LVDS218 receivers.

4.4.1.7 Ethernet interface

Ethernet data simulation for transmitting and receiving via normal RJ45 connector.

4.4.1.8 Optical interface

Payload data simulation for transmitting and receiving via optical interface device.

4.4.1.9 Digital IOs

32 Digital IOs which can be configured as input/output via GUI with Selectable voltage 3 to 28V.

4.4.1.10 Data processing

The data which is acquired/archived from UUT, has to be processed in real-time using hardware. Real-time processing for data rates up to 25 Gbps or better. The data has to be processed as per the CCSDS standard/ custom format as specified by the URSC.

5 Harness Fabrication:

Harness fabrication involves the wiring to connect UUT(IAP) with the test system and also to interconnect the instrumentations for controlling and data logging.

5.1 Harness realisation plan

5.1.1 All connections to be done on an Aluminium panel. Sample interconnection panel images are provided in figure.

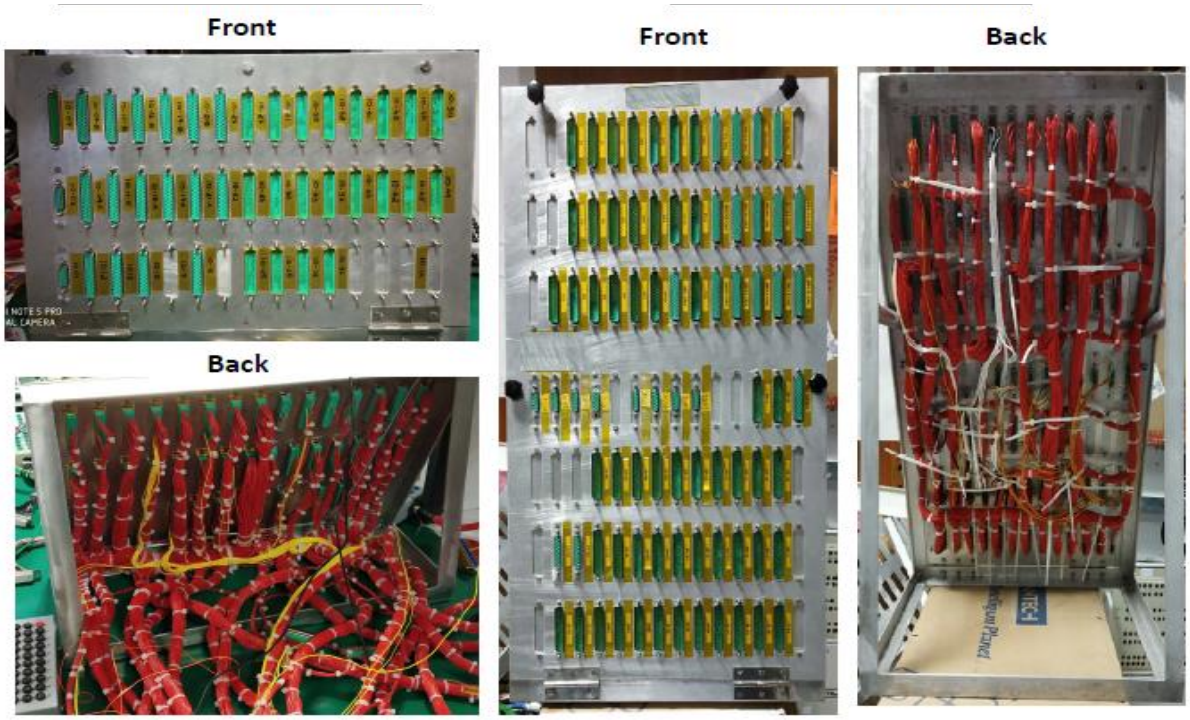


Figure 7: Inter connection panel

The Interconnection panel typically consists of 80No's of DSUB ITT 50 pin socket/plug connectors and 50 No's of DSUB ITT 78 pin socket/plug connectors. Number of Interconnections will be of the order 6000 contacts.

5.1.2 Suitable type of the harness to be provided to connect RF signals and high data rate signals as per the requirement.

	Type of signals	Connector type (Interface to UUT)	Remarks

5.1.3	LVDS, LVCP, SER/DES, RS485 and SPI	Gore/Sanghvi/Axon differential 100 Ω cables (3 Gbps Bandwidth).	
5.1.4	TLK2711	AXOMACH Connector TYPE10	
5.1.5	CMOS	Twisted Pair (Live and Ground)	
5.1.6	Mil-std-1553B	Mil-std-1553B cables with Stubs and termination.	
5.1.7	Ethernet	Twisted Pair (Live and Ground) as per 802.3 Std for 1Gbps and 10Gbps ethernet or LVDS.	
5.1.8	MGTs	Medium with bandwidth to support data rate of 20Gbps (TBD)	
5.1.9	Optical	TBD	

6 List of Deliverables for IAP test system:

The tentative list deliverables, which are required to realise test system modules are provided in the following table.

Sl.No.	ITEMS	Quantity	Type
Computers:			
1.	Host Work Station (LINUX)	4	Standard
2.	Industrial PC(LINUX)	3	Standard
3.	Industrial PC with chassis and motherboard, daughter board configuration	1	Standard
Rack and supply, current meter:			
4.	Industrial Rack Enclosure	3	Standard
5.	Power Supply (60V-25A) & (100V-15A)	1+1	Standard
6.	Console Power supply (triple output (0-30V & +/-15V supply)	2	Standard
7.	Panel Mounted Digital current meters	2	Standard
PC Based cards:			
8.	PCI based DAC card	3	Standard
9.	PCI Based Mil-std-1553 BC, Multi RT& MT simulator	1	Standard
10.	PCI based SPI and RS485 interface card	1	Custom made Vendor Design
11.	Xilinx based Digital I/O Hardware Simulation card	1	Custom made URSC Design
12.	PC based add-on card to simulate SPI/I2C/Discrete interfaces	1	Custom made Vendor Design
13.	PC based Encoder decoder card	1	Custom made Vendor Design
14.	Payload data Simulators-LVDS/LVCP/CMOS	1	Custom made Vendor Design
15.	Payload data simulator MGT interface	1	Custom made Vendor Design
16.	Payload data simulator Ethernet	1	Custom made Vendor Design
17.	Data serializer/ De serializer	1	Custom made Vendor Design
Stimuli units:			

Sl.No.	ITEMS	Quantity	Type
18.	Test Interface Package	1	Custom made URSC Design
19.	Interface Unit	1	Custom made URSC Design
20.	Sensor Stimuli Unit	1	Custom made URSC Design
21.	Heater & Thruster Load Unit	1	Custom made URSC Design
22.	GNSS signal source/record and replay	1	Standard
23.	Waveform Generator/Function Generator-Type1 (Lower data rate for TMTC)	1	Standard
24.	Waveform Generator/Function Generator-Type2 (Higher data rate for P/L data)	1	Standard
25.	Clock Source	1	Standard
26.	TTCP	1	Standard
27.	HSDR	1	Standard
28.	Up converter	1	Standard/Customized
29.	Down Converter type1	1	Standard/Customized
30.	Down Converter type2	1	Standard/Customized
Harness:			
31.	Mil-std-1553 Four stub coupler	4	Standard
32.	Ethernet Hub and cable assembly 10G	1	Standard
33.	Console Harness	1	Custom made
34.	RF cables and adaptors	1 set	Standard
Standard instruments			
35.	Spectrum analyzer	1	Standard
36.	Power Meter	1	Standard
37.	Directional Coupler	1	Standard
38.	Noise generator and attenuator	1	Standard
39.	Frequency counter	1	Standard
40.	RF cables and adaptors	1 set	Standard
41.	RF Attenuator	1	Standard
42.	RF selection matrix switch	1	Standard
43.	Multimeter with probes	2	Standard
44.	Digital Oscilloscopes (200MHz & 4GHz) with Differential probe and active probe	2	Standard
45.	Online monitor (OLM) (50 pin and 78 pin)	10+10	Standard
46.	Active OLMs	2	
47.	Current probe	1	Standard

Software:

1.	UI Software for SPS test with auto test features	1	Customized
2.	UI Software for BDH test with auto test features	1	Customized
3.	UI Software for RF test with auto test features	1	Customized
4.	Application programs / Device drivers for FEP SPS	1	Customized
5.	Application programs / Device drivers for FEP BDH	1	Customized
6.	Application programs / Device drivers for FEP RF	1	Customized
7.	Device drivers for all PC addon cards	For each PC addon card	Standard /Customized
8.	Software to control/Command/monitor instrumentation	For power supply/ current meter/ oscilloscope/ multimeter etc	Standard /Customized
9.	For OBC applications, it is preferred to run URSC software. Wherever Vendor not able to meet the URSC specified standard hardware, then software translation layers to be provided by the vendor	DAC/Mil-std-1553B/FPGA based DIO card software	Standard /Customized

7 Installation/Testing/Maintenance support:

7.1 Installation/ testing/ maintenance activities:

These test systems realised will be used across multiple projects. For each project assigned minor modifications shall be done based on the project requirements. Following are the Installation/Testing/Maintenance activities that shall be done for each project.

7.1.1 Test Harness modification / configuration for Project specific requirements.

7.1.2 Installation and Evaluation for Project specific requirements.

7.1.3 Preparation of Test plan, Inputs to test Procedures.

7.1.4 Test system support for Project activities

7.1.5 Vendor should carry out the installation and testing of the test system at URSC

7.1.6 Vendor should provide the testing support for the evaluation of UUT, which includes testing at various phases like IBT, Thermovac, EMI/EMC test, vibration test, FBT etc.

7.1.7 The work involves the integrated testing of the package with the test system delivered during the Initial bench test, shifting and making ready the setups for environmental tests and testing, and final bench test.

7.1.8 The work involves the setting up of the test system at various test beds, evaluation of the test console, debugging of the test console if any issues found.

7.1.9 Skilled manpower support will be required round the clock during certain critical phases of project activities

7.1.10 The Service Provider / Bidder shall abide by the law of the land including, Contract Labour (Regulation & Abolition) Act, EPF Act, ESI Act, Minimum Wages Act, Equal Remuneration Act, Employees Compensation Act, Payment of Wages Act, Income Tax Act, Goods and Service Tax Act and all labour related laws / Acts or any new regulations / legislation enacted in this regard and its compliance as applicable during the tenure of the Contract. Service Receiver shall in no way be responsible for any default regarding statutory obligation. The Service Provider / Bidder has to ensure compliance of the above provisions at the time of submission of bill to the Service Receiver and while making payments to their work-force at all times during the currency of the Service Contract.

7.1.11 Test report generation.

7.1.12 Based on the Installation/maintenance/test support required, schedule will be provided by URSC through work order, Vendor has to support the activity. The same is to be implemented without any slippage within 15 days of receiving the work order.

7.1.13 Payment for installation/Maintenance/operation support is based on time to time execution of work, based on work order generated.

8 Responsibility Matrix:

Responsibility matrix during the various phase of realisation are provided below.

8.1 Test system Initial phase

Phase	Sl No	Activity	ISRO responsibility	Vendor responsibility
Test system Initial phase	1.	Electrical Interface for Test System	Y	
	2.	UI software requirement	Y	
	3.	Application software for FEP requirement	Y	
	4.	Integrated test system software requirement	Y	
	5.	FPGA requirement	Y	
	6.	Test automation requirement	Y	
	7.	Data storage and archival requirement	Y	
	8.	ICD for non-standard interface	Y	
	9.	Schematic in pdf format for URSC design	Y	
	10.	Schematic generation for URSC design		Y
	11.	Schematic generation for vendor design		Y
	12.	Schematic review	Y	Y
	13.	Specifications for standard units	Y	
	14.	Source for the standard equipments and the consent from the respective supplier		Y
	15.	Compliance for the standard units wrt specifications provided		Y
	16.	Review of compliance matrix for standard instruments	Y	Y
	17.	EID for harness fabrication	Y	
	18.	Harness fabrication plan and details		Y
	19.	Harness fabrication plan review	Y	Y
	20.	Assembly plan for test system units		Y
	21.	Assembly plan for test system units Review	Y	Y

8.2 Test System Design phase

Phase	Sl No	Activity	ISRO responsibility	Vendor responsibility

Test System Design phase		Software design for UI		Y
		Software design review for UI	Y	Y
		Application software design for FEP		Y
		Application software design review for FEP	Y	Y
		Integrated software design		Y
		Integrated software design review	Y	Y
		FPGA design		Y
		FPGA design review	Y	Y
		Test automation realisation		Y
		Review of test automation realisation	Y	Y
		Data storage and archival implementation		Y
		Review of Data storage and archival implementation	Y	Y
		PCB layout design for both URSC designed and vendor designed boards		Y
		Harness realisation and testing		Y
		Harness test results review	Y	Y

8.3 Test System realisation Phase

Phase	Sl No	Activity	ISRO responsibility	Vendor responsibility
Test System realisation Phase		Unit level testing of SW (UI and application)		Y
		Integrated testing of SW		Y
		Component procurement		Y
		Package fabrication		Y
		Testing of individual boards / units		Y
		Test results verification for individual boards / units	Y	Y
		Integrated test system software review	Y	Y
		Integration of test system hardware and software		Y
		Integrated test system T&E		Y
		Integrated test system T&E results review	Y	Y

8.4 Test System Installation/maintenance /operation support

Phase	Sl No	Activity	ISRO responsibility	Vendor responsibility
Test System Installation/maintenance /operation support		Installation		Y
		Configuring test system for a project		Y
		Review of Configuring test system for a project	Y	Y
		Maintenance		Y
		Operation support	Y	Y

9 Documents to be furnished along with RFQ

Sl No	Particulars	Remarks
9.1.1	Completed point by point compliance matrix 2.1 to 2.3 3.1 to 3.2 4.1 to 4.4 5.1 to 5.2 6 7.1 to 7.10 8.1 to 8.4 ,9,10,11	
9.1.2	Willingness to sign non-disclosure agreement with ISRO	No data shared by ISRO shall be re-shared. No data generated by the vendor towards this development shall be shared to any party other than ISRO.
9.1.3	List of chosen facilities for fabrication and letter of acceptance by facility provider to provide the facility	
9.1.4	Detailed project management structure to execute the activity	Manpower allocation for each position shall be provided. Whether internal employee or a consultant shall be mentioned. Experience of the manpower with documentary proof of experience.
9.1.5	Detailed Project schedule	
9.1.6	For the standard products, willingness from the respective vendor and compliance to the requirements	

10 Vendor Evaluation criterion

The vendor selection is a process to ensure that only industries with the capability to carryout embedded systems with RF, mixed signal, high speed digital and mechanical designs are part of the further process.

A detailed list of the vendor qualification criterion is provided in the table 8.1 which needs to be provided by all the interested industries. These responses will be evaluated by URSC and those vendors who are able to provide all the data and proofs for meeting all the criterion only will be selected for further process.

Table 10.1: Vendor qualification criterion

Sl.No	Criterion	Proof	Remarks
1	Experience in developing test setups with embedded h/w and s/w	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
2	Experience with PCB design with high density ground FPGA	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
3	Experience in working with LINUX OS	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
4	Experience in developing UI software	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal

5	Experience in developing embedded software	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
6	Experience in developing FPGA codes and application	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
7	Experience in developing applications for MIL-std-1553B bus (BC MRT MT)	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
8	Experience working with real-time systems	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
9	Experience in testing the avionics systems	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal

10	URSC requires all technical data to be shared by vendor for review and documentation.	Compliance to be provided	Reports shall be attached along with the proposal
11	Vendor shall sign a Non-Disclosure agreement with URSC after PO release.	Compliance to be provided	Compliance certificate
12	Experience in developing applications for SPI,I2C	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
13	Experience in developing applications with Ethernet interface	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
14	Hardware compliance	Compliance to be provided for hardware against each specification	Detailed specifications/ user manuals/Data sheet reference for each specification
15	Experience in developing RF test systems	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal
16	Experience in developing SPS test systems	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the	Reports shall be attached along with the proposal

		requirement	
17	Experience in developing test systems for High bit rate data handling systems	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement	Reports shall be attached along with the proposal

For serial No.s 15-17 if vendor is willing to have collaboration , should produce consent letter from the party , with whom they are planning to collaborate, and also required to produce Purchase order with a certification for successful completion OR to produce a product present in that company's catalogue /website meeting the requirement .

All the units are evaluated against the technical specification whether custom built or standard. Orders will be placed on technically suitable L1.

11 EOI process and statement of work

Expression of Interest (EOI) for identifying a suitable vendor for joint development of IAP test system will have a Pre-bid meeting where interested vendors will be briefed regarding the process as detailed in figure 1.

A detailed vendor selection criterion is provided in this document, for which prospective vendors are required to provide all the documentary proofs as per the list. All responses will be evaluated by URSC and a list of probable vendors will be selected.

List of deliverables and details required to make a proposal is provided in this EOI. Based on the data, vendor is expected to give an engineering proposal with all technical details along with project execution plan. A presentation from vendor may be sought to understand the proposal.

All received proposals will be evaluated based on a pre-defined criterion mentioned in this document, and list of selected vendors will be generated. An indenting process will be initiated in a Limited tender mode only on those vendors whose EOI is selected. A flow chart of the process is as shown in Figure 7.

11.1 Statement of Work

This section provides a brief idea of the total work to be carried out by the vendor after receipt of purchase order. The complete project is divided into 3 phases.

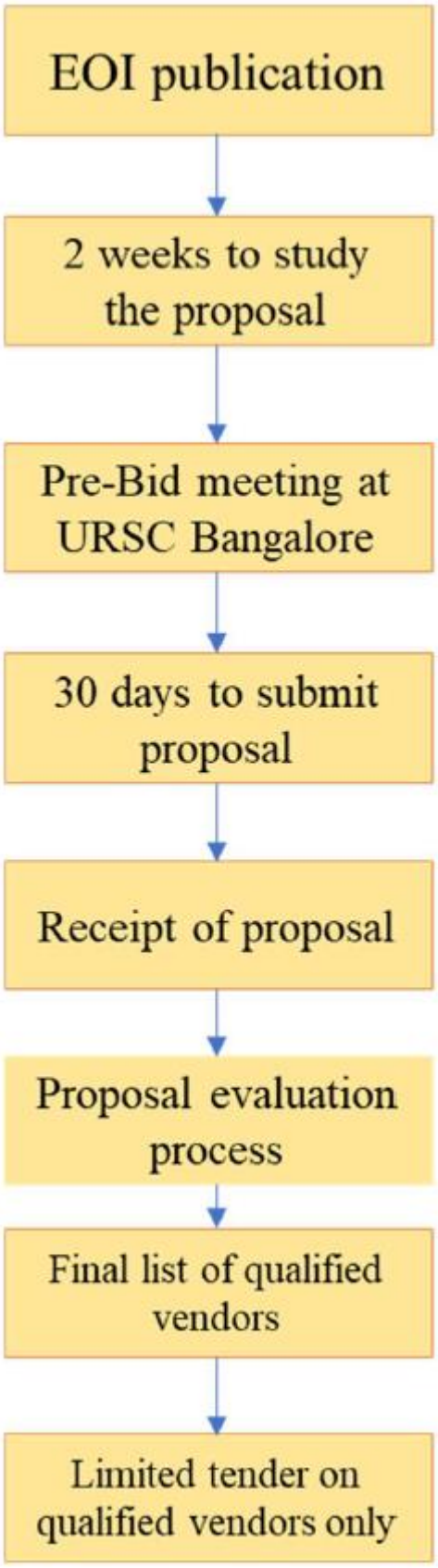


Figure 8: Process flow

11.1.1 Initial phase

Initial phase starts after the PO is placed and NDA (Non-Disclosure Agreement) is signed between vendor and URSC.

Test system architecture, Major specifications of the test system boards, FPGA and software requirements, schematic design wherever applicable will be provided by URSC. Any suggestions or improvements can be proposed by vendor. Final decision to accept the proposal in part, total or to reject it is at URSC discretion.

Vendor needs to carry out initial assessment of the test system. After design finalization by the vendor, a joint Preliminary Design Review (PDR) will be held by vendor to obtain clearance from URSC.

Following aspects shall be discussed at the PDR stage:

- Test system configuration
- Schematic design for vendor responsible design
- Software architecture
- FPGA design capture
- Test plan for Automated test
- Project execution plan and schedule
- Plan for Installation/ test support/ maintenance
- Documentation
- Harness fabrication

11.1.2 Design phase:

- After clearance from URSC, the vendor shall initiate test system development followed by below mentioned activities
- After all the design objectives are met, vendor shall hold a joint Detailed Design Review (DDR) with URSC to obtain the clearance to proceed further.
- DDR shall include review of the following activities
  - PCB design placement and routing
  - Review of schematic changes if any
  - Software requirements
  - FPGA simulations
  - Test system adequacy
  - Test case list for test system evaluation
  - Fabrication process
  - Project plan and schedule
- DDR clearance is a mandatory requirement to continue further activities

11.1.3 Realisation phase:

- Vendor shall carry out the complete development of test system including board design, software and FPGA development, Harness fabrication.
- Vendor shall provide the test documents
  - Design document of individual units of the test system
  - Test results for individual units of the test system
  - Test results for Integrated test setup
  - Integration document of the test setup
  - Harness details

    - Software test document
    - Software design document
    -
    -
- Any issues observed during the testing need to be addressed, resolved and reviewed. If required parts to be replaced.

11.1.4 Installation / maintenance and operation support phase:

These test systems realised will be used across multiple projects. For each project assigned minor modifications shall be done based on the project requirements. Following are the Installation/Testing/Maintenance activities that shall be done for each project.

- Test Harness modification / configuration for Project specific requirements.
- Reworks / reconfiguration carried out to be presented to the URSC review committee
- Installation and Evaluation for Project specific requirements.
- Preparation of Test plan, Inputs to test Procedures.
- Test system support for Project activities
- The installation and testing of the test system at URSC at various test beds
- Vendor should provide the testing support for the evaluation of UUT, which includes testing at various phases like IBT, Thermovac, EMI/EMC test, vibration test etc.
- Integrated testing of the package with the test system delivered during the Initial bench test, shifting and making ready the setups for environmental tests and testing, and final bench test.
- Setting up of the test system at various test beds, evaluation of the test console, debugging of the test console if any issues found.
- Test report generation.
- Any issues observed during the testing need to be addressed, resolved and reviewed. If required parts to be replaced.

12 Annexure A

12.1.1.1 Standard Components:

Host Workstation:

Host work station implements all the necessary software to communicate and operate all the units of the test system. The software provides the function of configuring all test system units, sending and receiving data, data archival, retrieval and display in real time/offline, simulation of spacecraft dynamic environment etc.The workstation shall run on Linux platform and shall meet the specifications as given in Section. The minimum required specifications are listed below-

- Processor with 16 or more cores
- 64 GB DDR4 or better RAM
- Two 2 TB storages with RAID support
- RTX 20 series with 8 GB GDDR6 or better GPU
- RED HAT ENTERPRISE Linux operating system
- Multiple USB and 1/10G Ethernet ports

12.1.1.2 Rack Enclosure:

All components of the test system are to be assembled in a standard DIN 41494, 36U-19" rack. It should be portable and capable of distributing power to all the units assembled inside.

12.1.1.3 Power Supply:

A power supply module is needed to feed regulated and differing levels of power to the Avionics Package. TDK-Lambda power supplies of the model *GEN60-25A/1500W-1U and GEN100V-15A/1500W-1U are* preferred. Remote access and control features are required.

12.1.1.4 Console Power Supply:

A triple output supply is needed to power ON test system units or any I/O modules. Following are voltage and current rating required.

No	Specifications	32V/2A	± 15V/0.5A	5V/5A
1.	Input Voltage	230V AC, ± 10%,50Hz,1Ø supply		
2.	Output Voltage	0 – 32V	12V-15V	5±0.5V
3.	Output Current	0-2A	0-0.5A	0-5A

12.1.1.5 Panel Mounted Digital Current meters:

The digital current meters are responsible for monitoring the current from the UUT. Functional requirements of the meters are listed below:

- Digital current display with LED.
- Accurate up to 5 digits i.e. 99.99% at full scale.
- Current range- 5A DC with maximum 0.04% error at full scale.
- RS-485 interface for reading the current value.
- Isolated analog output channels.
- Provision to capture minimum, maximum, and average output current values.

12.1.1.6 Industrial Computer:

The 19" rack mountable industrial computer is responsible for housing the PCI based D/A boards, MIL-STD-1553B boards, SPI & RS485 interface boards, and Xilinx FPGA based digital I/O simulation board. It coordinates tasks through these boards to support TC-TM interfaces, MIL-STD-1553B BC-RT communications, and digital I/O simulations. The required specifications are listed below:

- CPU with a core count of 12 or higher.
- 8GB DDR4 RAM or better, expandable up to 16 GB.
- 512 GB or larger SSD.
- 20 or more full size slots including 14 or more PCI slots.
- OS- RED HAT Linux 6 or higher with licensed CD/DVD media.

<u>Chassis Specification for BDH/SSR Industrial computer</u>

- No.of slots – 16 or better
- Per slot Bandwidth –1GB/s or better
- Form factor – 4U 19" rack mountable
- Cooling – forced air cooling with inbuilt fans
- Chassis should meet international safety standards related to electrical equipment and EMI/EMC standard.

12.1.1.7 PCI based 16 channel D/A boards:

The 16 channel D/A boards provide programmable analog voltage and current output signals along with digital control and data signals. ICP DAS PIO-DA16 cards are preferred. Its functional requirements are listed below:

- 16-channel double buffered analog outputs. Each channel should be capable of being selected to output voltage/current signals.
- The output type (unipolar/bipolar) and range should be programmable through software.
- It should have 16 TTL-level digital inputs and outputs.
- It should have a Quad14-bit MDAC.
- Driver and application software (APIs) built on RED HAT Linux are to be provided along with the board.

12.1.1.8 PCI based MIL-STD-1553 simulator card:

The MIL-STD-1553 simulator card simulates 1553 bus communication with the UUT for data acquisition, commanding, and data monitoring applications. Cards similar to BU-67210i200R-JL0 are preferred. The functional requirements are listed below:

- Should support two dual redundant multi-functional MIL-STD-1553 A/B channels.
- Each 1553 channel should be capable of simulating BC, multi-RT, and MT functionalities concurrently.
- Each channel should be accessible through separate independent applications running on the computer simultaneously.
- Should be capable of simulating up to 31 RTs with software programmable RT addresses on a single channel.
- Should provide eight or more user programmable discrete digital I/Os.
- Linux based device drivers and software APIs are to be provided along with example scripts for BC/RT/MRT/MT modes with individual and combined applications. All functions should be software configurable.
- The software should have provision to inject errors through the BC messages and RT responses.

12.1.1.9 PCI based SPI and RS485 Interface card:

Hardware requirements:

- Needs to support communication through 20 or more differential 4-wire SPI channels simultaneously and independently from each other.
- Voltage level should be LVDS/LVCMOS.
- Power supply to the card ought to be switchable between the PC and external power through jumper.
- Should have configurable active-high/active-low chip-select.
- Capable of operation at clock speeds in the range of 1-12 MHz.
- Each SPI channel should have a dedicated memory space allocated for buffering the communicated data temporarily.

Software requirements:

- Driver software should be compatible with RED HAT Linux 6 or higher versions.
- All SPI channels should be independently configurable through the software as master/slave. Each channel should support configurable clock speeds and all 4 SPI modes for communication. The transaction width (8 bits / 16 bits) should also be software configurable.
- The driver software would handle send and receive events of each channel in an interrupt context independently.

- The driver needs to take care of constructing, de-constructing, and routing the frames communicated through PCI to and from the individual channels with proper headers for identification of channels.
- Software APIs are to be provided for configuration, initialization, and communication processes along with example scripts and explanations.
- Software APIs are to be provided to
    - Receive data from HOST workstation over Ethernet for sending it to UUT through SPI.
    - Send the received data from UUT through SPI over Ethernet to HOST.

12.1.1.10 PCI based RS485 interface card:

Hardware requirements:

- Needs to support communication through 15 or more RS-485 channels simultaneously and independently from each other.
- Voltage level should be LVDS/CMOS.
- Power supply to the card ought to be switchable between the PC and external power through jumper.
- Capable of operation at max speeds of 5 Mbps.
- Each channel should have a dedicated memory space allocated for buffering the communicated data temporarily.

Software requirements:

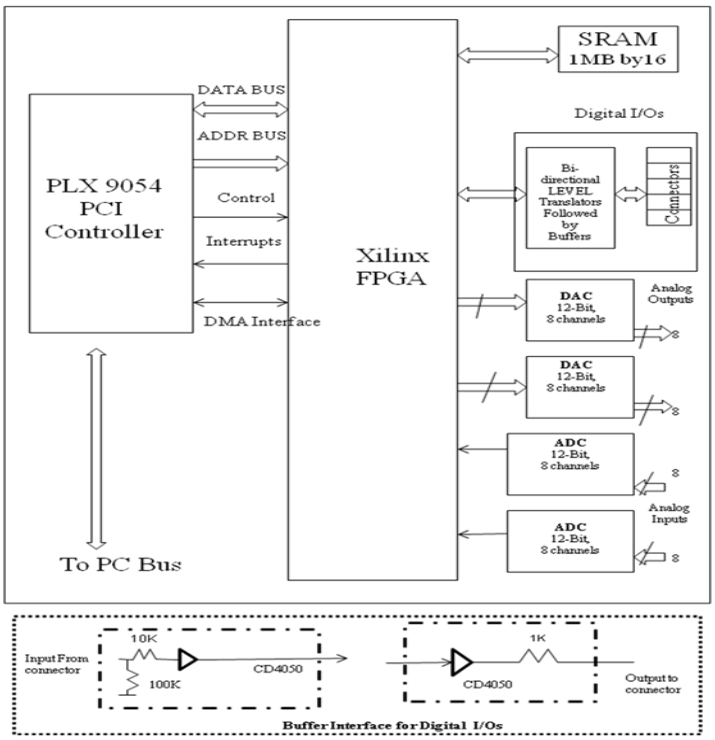
- Driver software should be compatible with RED HAT Linux 6 or higher versions.
- All channels should be independently configurable through the software regarding baud rate, Parity and stop bits.
- The driver software would handle send and receive events of each channel in an interrupt context independently.
- The driver needs to take care of constructing, de-constructing, and routing the frames communicated through PCI to and from the individual channels with proper headers for identification of channels.
- Software APIs are to be provided for configuration, initialization, and communication processes along with example scripts and explanations.
- Software APIs are to be provided to
    - Receive data from HOST workstation over Ethernet/USB for sending it to UUT.
    - Send the received data from UUT over Ethernet/USB to HOST.

12.1.1.11 PCI based Xilinx FPGA card for digital I/O simulation:

Hardware Requirements:

- I/O should be 5V compatible and tolerant.

- There should be provision to switch the power supply to the card between the pc and external power supply through jumper.
- The card should be developed around a high-density Xilinx FPGA. FPGA programming and development tool are to be provided. The FPGA should be programmable upon power up through PROM.
- The I/O lines are to be distributed among three cards. The main card would contain the FPGA along with other necessary ICs for configuring the lines depending on the application. An input and an output card would buffer the input and output signals routed through the connectors.
- A total of 256 user configurable I/O lines (128 I/P and 128 O/P) are to be implemented.
- Communication between the PC and the FPGA would be executed through PCI.



Software requirements:

- Linux based driver software needs to be developed for communicating with the FPGA through PCI.
- It should be capable of supporting TM-TC interface, RMU interface, Pulse Per Second (PPS) interface, etc.

12.1.1.12 Test Interface Package (TIP):

Test interface package (TIP) performs the function of sensing, measuring, and forwarding command outputs from the UUT. A block diagram representing the module is shown in figure 2. Functional aspects of the module are as follows-

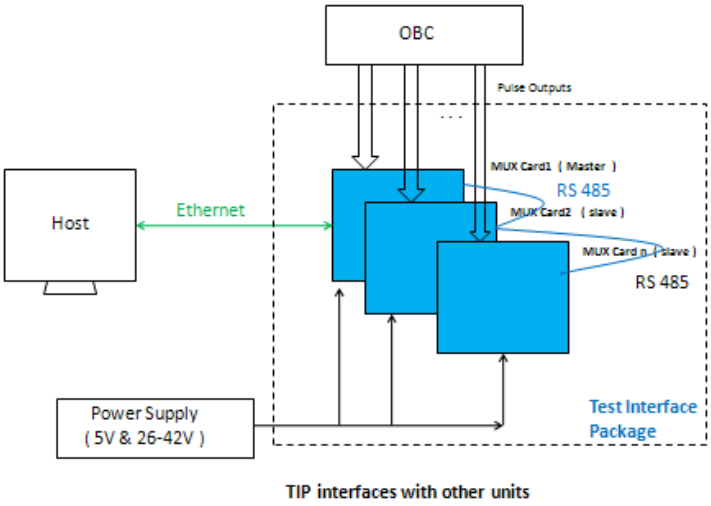


Figure 2:Block diagram representing the Test Interface Package

Functional requirements:

- The unit consists of6 identical multiplexer cards interconnected through a back-plane motherboard and housed in a 7U or less Euro sub-rack. The package should function with a minimum of 1 and a maximum of 6 mux cards to test various types of pulses and level signals from the OBC.
- The signals captured from the UUT through the connectors are to be measured, processed, and forwarded to the industrial computer through ethernet.
- A suitable protocol for command and data transfer through the ethernet would be finalized post-consultation with URSC.
- Design should be using a high-density FPGA / Microcontroller, with a resettable 12-bit milli second counter.
- Each card should support serial RS-485 and Ethernet (100 MBPS) interface communication. The Cards should be configurable as a Master or as a Slave through jumpers. As a master it should receive commands from the host through ethernet and transfer its own data along with the data acquired from the slave mux cards back to the host. Communication between the master and slave cards should be through serial RS-485. The package should not function if more than one card is configured as a Master.
- Every 1 sec TIP should provide pulse width, number of pulses along with the time stamping information to the host with a START command from TIP.
- Suitable CMOS buffers, Schmidt trigger gates and level shifters should be employed if necessary for accurate processing of the incoming signals.
- Types of signals to be processed-
  A total of 188 parallel pulse and level signals etc. are to be processed-

- 80 5V pulse signals.
- 7 5V level signals.
- 8 current-input opto-coupler interfaces.
- 40 high voltage (26-42 V) Raw Bus (RB) pulse signals.
- 4 high voltage (26-42 V) RB level signals.
- 20 5V data command transfer pulses.
- 2 EED open collector interfaces (high voltage with pull-up).
- 6 differential command interfaces.
- 10 5V data command clocks.
- 10 5V data command data signals (32-bit).
- 2 Snap interfaces.

12.1.1.13 Interface Unit (IU):

The Interface Unit simulates various digital and analog interfaces for the UUT. The functional requirements are listed below-

- The unit should be realized through a mother-board daughter-board concept. There should be 8 daughter-boards in total with each daughter-board providing a designated type of stimulus.
- The stimuli are to be controlled and accessed through a serial interface of 8-bit data, clock, and transfer pulses.
- The mother and daughter boards are to be housed in a 6U aluminium structure of 19" width.
- Types of stimuli to be implemented-
  - Digital I/O interfaces (0/5 V): 288
  - RF-bit interfaces (0 V/open): 96
  - Analog channels (range- ±5 V): 147
  - Thermistors: 288
  - Data transmitters: 8
  - Data receivers: 8

12.1.1.14 Sensor Stimuli Unit:

The sensor stimuli unit's task is to provide suitable voltage/current/resistance stimulus to the sensor interfaces of the UUT for simulating its environment. The General requirements of the unit are listed below-

- The unit should be realized through mother-board daughter-board concept. It should house 8 daughter-boards with each board responsible for generating a designated type of stimulus.
- The stimuli and the cards are to be controlled and generated through 16-bit digital data commands or analog inputs to the unit.
- The cards should be enclosed in a 6U aluminium cage of 19" width.

- Types of stimuli to be generated-
  - Magnetometer (±30 mA): 2
  - 4-Pi sun sensors (±10 mA): 2 (12 stimuli per sensor)
  - Platinum resistance temperature (PRT) sensors (resistance): 60 (8 values per sensor)
  - Thermocouples (0-40 mV): 40
  - Fine temperature sensors (FTS) (resistance): 60 (8 values per sensor)
  - Coarse analog sun sensors (CASS) (±10 uA): 16
  - Solar panel sun sensors (SPSS) (±10 mA): 16

12.1.1.15 Heater and Thruster Load Unit (HTLU):

The HTLU provides resistive loads for all the high voltage command interfaces and on/off status monitoring. Following are the functional requirements of the unit-

- The unit should be realized through a mother-board daughter-board concept. The connection between the mother-board and the daughter-boards should be intact even when the daughter-board gets pulled out from the tray.
- The unit needs to simulate 4 types of loads- Heaters, Latch valves & ILV, Magnetic torquer coils (MTC), and Thrusters & LAM.
- 432 heater loads of different wattages are to be simulated for 42 V Raw Bus lines. The status of the loads is monitored at the output of opto-couplers (0/5 V).
- 10 loads of LV with positive and negative pulse (28-42 V pulses) and 35 loads of ILV with positive pulse monitoring to be implemented. Channel selection is done through telecommand interface.
- 6 units of MTC loads across 42 V are to be provided. These loads are subjected to bidirectional current stimuli from the UUT.
- 18 thrusters and 2 LAM loads capable of dissipating 75 W across 42 V should be implemented. Operational status of these loads should be indicated through LEDs on the front panel.

12.1.1.16 GNSS signal source

The RF source to test and evaluate the performance of SPS can be a GNSS Simulator or GNSS record and replay or a Vector Signal Generator witha GNSS Simulator feature.
These instruments are available commercially off the shelf.

The instrument shall be capable of the following:

- Multiple GNSS Constellation: GPS, NavIC/IRNSS and Galileo
- Capability to test multi-frequency bands (L1, L2 and L5)
- Configurable power levels to simulate weak or strong signal.
- Support for custom trajectory generation.
- Real-time and pre-recorded signal playback.
- RF environment Simulation
- Interference and robustness testing

12.1.1.17 Clock Source:

- A Temperature Controlled Crystal Oscillator (TCXO) or external clock to calibrate the Pulse Per Second (PPS) with an accuracy of ±50ns.
-

12.1.1.18 PC Addon card for OBC interface simulation Test System

PC addon card to simulate the following interfaces

- I2C (Inter-Integrated Circuit),
- SPI (Serial Peripheral Interface),
- Discrete DIO to generate pulse commands/level commands and to read the discrete input lines.
- FPGA based PC Addon card with the above-mentioned interfaces
- FPGA design
- Software design
- Voltage Level Shifter for 5V to/from 3.3V conversion

The board operates as the master, and the SPS functions as the slave.

- SPI:It is configured as Master which is configured and operated through Ethernet
  - Supports four-wire SPI interface (SCLK, SS, MOSI, MISO)
  - Configurable SCLK Frequency – 1MHz to 12MHz
  - Configurable Big-Endian / Small-Endian
  - Configurable SPI Mode – 0/1/2/3 operation
  - Configurable Data Size per transaction
  - In addition to the standard 8-bit word length (used in INS), the SPI slave shall support 16-bit word lengths.
- I2C: The I2C master initiates communication with slave connected to the I2C bus configured and operated through Ethernet interface. The following functions to be supported:
  - Two-wire interface (SDA, SCL)
  - Configurable 7-bit (used in INS) and 10-bit Addressing Mode
  - Configurable bus speeds: Fast-mode, Fast-mode Plus, High Speed mode (optional)
  - Supports Clock stretching
  - Integrated Pull-up
  - Integrated Glitch filter
  - Arbitration lost detection in multi-master system (optional)
- 64x Digital Inputs and 64x Digital Outputs with the below features which is configured and operated through ethernet interface.
  - Configurable Single ended (3.3V/5V) and differential (LVDS 2.5/3.3) operation
  - Frequency & Duty Cycle Measurement on Digital Input Pins
  - Configurable Digital Outputs with:
    - Value Deposit (Either High/Low)

- PWM Signal with Frequency (1Hz to 4MHz) and Duty Cycle (10% to 95%)

12.1.1.19 SPS Application software:

FEP Application Software

A. The FEP is connected HOST COMPUTER through ethernet interface.
B. Driver software for addon cards and application programs to configure them to be provided.
C. Applications in FEP should receive the command from HOST GUI and accordingly carry out the functions.

The application software runs on the HOST COMPUTER must be capable of continuous data logging without user intervention. The file format for storage are both

HOST COMPUTER GUI Software

a) Receives logged data from the FEP and displays it in a user-friendly interface on the HOST COMPUTER.

b) Provides tools for data analysis, visualization, and logging for further processing.

c) The software should be user-friendly, flexible, and compatible with the programming languages and development environments used in the testing application.

12.1.1.20 TTCP

- It is required for generating modulated signal, demodulation of TM data, TC threshold, BER measurement and constellation monitoring.
- Preferred frequency: direct RF; 70MHz with associated upconverter/downconverter is also acceptable
- Should support following modulation and demodulation schemes:

  Direct modulation: BPSK, QPSK, DSSS-BPSK(CDMA), DSSS-QPSK(CDMA)

  Sub carrier based: PCM/PSK/PM, PCM/PSK/FM
- Should support tone and PN ranging
- Should support different coding schemes (convolution, RS, Turbo etc).

12.1.1.21 HSDR 4G+ supporting FACM

- It is required for BER measurement and constellation.
- HSDR required
- Patch for FACM demodulation
- Should support various channel coding schemes

- Should support demodulation of All supported modulation schemes and FACM

12.1.1.22 Up-Converter

- This is required for conversion of 70 MHz signal to S/X-band RF signal.
- S-band frequency range: 2.0 to 2.12 GHz
- X-band frequency range: 7.145 to 7.25 GHz
- This is not required if TTCP supports direct RF frequency.

12.1.1.23 Down-Converter type-1

- This is required for conversion of S/X-band RF signal to 70 MHz to make it compatible with TTCP.
- S-band frequency range: 2.2 to 2.3GHz
- X-band frequency range: 8.4 to 8.5 GHz
- This is not required if TTCP supports direct RF reception

12.1.1.24 Down-Converter type-2

- This is required for conversion of X/Ka-band RF signal to 720/1200 MHz to make it compatible with HSDR.

12.1.1.25 Spectrum Analyser

- It is required for measurement of RF spectrum at S/X/Ka-Band.
- RF power handling capability of more than 30 dBm.
- The frequency span: 0 to 32 GHz
- Preferred to have analog demod option enabled.

12.1.1.26 Power Meter

- It is required for measurement of RF power at S/X/Ka-Band.
- RF power handling capability of more than 30 dBm.

12.1.1.27 Data/ Waveform Generator

Type-1

- This is required for external TM Data generation
- The TM Data is typically:
- Square wave: frequency: 1KHz to 10MHz, Level: 0 to 5V, 50% duty cycle
- PRBS Type: frequency: 1KHz to 10MHz, Level: 0 to 5V, 50% duty cycle, PRBS-7/11/15

Type-2

- This is required for external Data generation
- The Data is typically PRBS Type: frequency: 1KHz to 500MHz, PRBS-7/11/15 (I & Q data generation with LVDS)

12.1.1.28 Directional Coupler

- It is required for splitting RF signal and distributing it to multiple equipment for simultaneous monitoring.
- Frequency Range: 2-18 GHz
- Coupling Factor: 10 dB+/- 1 dB
- Power Handling capability: 2 Watt (Min)

12.1.1.29 Noise Generator

- To add noise on the modulated signal with required noise density (max noise density ≥ -126 dB/Hz
- Provision to attenuate the RF signal/Noise signal

12.1.1.30 Frequency Counter

- Frequency Range: up to 12 GHz

12.1.1.31 RF Cables and Adaptors

- Cables and adapters required for interconnections between CBSP and equipment
- RF attenuators to test the dynamic range of receiver.
- Frequency Range: S/X/Ka-band
- Adapters for connector end power measurement.

12.1.1.32 RF Attenuator

- For adjusting dynamic range for receiver test
- Upto 100 dB attenuation in steps of 1 dB and 10 dB.

12.1.1.33 PC based addon card for Encoder and decoder simulation

- This is required for generation and execution of telecommands.
- Encoder has to generate the TC frame along with idle pattern with defined time gap between each TC.

- Decoder has to accept data, clock and lock indication from DUT and verify the execution of commands generated by encoder. It has to provide the count of executed no. of commands.

12.1.1.34 IPC with automated console

- IPC to house the PC addon cards for commanding RF Systems from OBC To select modulation scheme, coding scheme, To select between internally generated data/ OBC data, record, Playback, RT and NRT modes, PN playback, Data bypass mode, Channel on/off.

12.1.1.35 RF selection matrix switch

- Frequency Range : 0.4-30 GHz
- Return loss of all ports: Better than 15dB
- Isolation between ports : Better than 70dB
- Power Handling : 1W CW
- Switching time: 20 msec max (break before make)

12.1.1.36 LVDS interface simulators:

- Payload Data simulation with LVDS transmitters.
- Data acquisition through LVDS receivers.
- Simulated data patterns should include file based multiple images , incremental, decrement, PRN15, 0x00FF, 0xFFFF, 0x0000, 0xAA55, 0x55AA data.
- User defined data pattern loading through file.
- Configurable interface related parameters. Ex: ON/OFF width, signal toggling edge.
- Programmable clock up to 400MHz for data generation and acquisition.

12.1.1.37 LVCP interface simulators:

- Payload Data simulation with LVCP transmitters.
- Simulated data patterns should include file based multiple images, incremental, decrement, PRN15, 0x00FF, 0xFFFF, 0x0000, 0xAA55, 0x55AA data. User defined data pattern loading through file.
- Configurable interface related parameters. Ex: ON/OFF width, signal toggling edge.
- Programmable clock up to 1000MHz for data generation
- FPGA Fabric based SER interface simulation.

12.1.1.38 MGT interface

- Payload Data/Ethernet data simulation with MGT transmitters.
- Payload Data/Ethernet data acquisition with MGT receivers.
- Simulated data patterns should include file based multiple images , incremental, decrement, PRN15, 0x00FF, 0xFFFF, 0x0000, 0xAA55, 0x55AA data.
- User defined data pattern loading through file.
- Programmable data rate up to 12.5Gbps.
- Configuration of MGT as transmitter/receiver/both using GUI.

12.1.1.39 CMOS interface

- Payload Data simulation with CMOS transmitters and data acquisition through receivers.
- Simulated data patterns should include file based multiple images , incremental, decrement, PRN15, 0x00FF, 0xFFFF, 0x0000, 0xAA55, 0x55AA data.
- User defined data pattern loading through file.
- Configurable interface related parameters. Eg. ON/OFF width, signal toggling edge.
- Programmable clock up to 10MHz.
- Should have provision to support 3.3V/5V output.
- Should have provision for CMOS interface using HCT244 for higher drive strength.

12.1.1.40 TLK2711

- Payload Data simulation with TLK2711 transmitters.
- Payload Data acquisition with TLK2711 receivers.
- Simulated data patterns should include file based multiple images , incremental, decrement, PRN15, 0x00FF, 0xFFFF, 0x0000, 0xAA55, 0x55AA data.
- User defined data pattern loading through file.
- Programmable data rate up to 2.5Gbps.
- Configuration of TLK2711 as transmitter/receiver using GUI.

12.1.1.41 LVDS SERDES

- Payload Data simulation with LVDS217 transmitters.
- Payload Data acquisition with LVDS218 receivers.
- Simulated data patterns should include incremental, decrement, PRN15, 0x00FF, 0xFFFF, 0x0000, 0xAA55, 0x55AA data.
- User defined data pattern loading through file.
- Programmable data rate up to 1.5Gbps.

12.1.1.42 Ethernet interface

- Ethernet data simulation for transmitting and receiving via normal RJ45 connector.

- Simulated data patterns should include incremental, decrement, PRN15, 0x00FF, 0xFFFF, 0x0000, 0xAA55, 0x55AA data.
- User defined data pattern loading through file.
- Programmable data rate up to 1/10Gbps.

12.1.1.43 Optical interface

- Payload data simulation for transmitting and receiving via optical interface device.
- Simulated data patterns should include incremental, decrement, PRN15, 0x00FF, 0xFFFF, 0x0000, 0xAA55, 0x55AA data.
- User defined data pattern loading through file.

12.1.1.44 Digital IOs

- 32 Digital IOs which can be configured as input/output via GUI.
- Selectable voltage 3 to 28V.

12.1.1.45 Data Generation

- Data to UUT has to be generated by the test console as specified in S.N 12.1.1.37 to 12.1.1.46.
- Data Acquisition
- Data from UUT has to be acquired in a PC and archived for data rates up to 25 Gbps or better.

12.1.1.46 Data processing

- The data which is acquired/archived from UUT, has to be processed in real-time using hardware.
- Should support real-time processing for data rates up to 25 Gbps or better.
- The data has to be processed as per the CCSDS standard/ custom format as specified by the URSC.