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No: EOI/AOEP/2025/07-2-25/शुद्धिपत्र

21 फरवरी 2025

प्रिय महोदय,

एड्रिन ऑनबोर्ड एम्बेडेड पैकेज (AOEP) के लिए "रुचि की अभिव्यक्ति" [EOI] के लिए आमंत्रण

उन्नत आंकडा संसाधन अनुसंधान संस्थान (ADRIN) अंतरिक्ष विभाग, भारत सरकार के अंतर्गत एक AOEP (एड्रिन ऑनबोर्ड एम्बेडेड पैकेज) विकसित करने की योजना बना रहा है। जैसा कि हमारे "रुचि की अभिव्यक्ति" [EOI] आमंत्रण में उल्लेख किया गया है, AOEP (एड्रिन ऑनबोर्ड एम्बेडेड पैकेज) बोर्ड के विकास में हार्डवेयर, सॉफ्टवेयर, फर्मवेयर, बोर्ड निर्माण, तीसरे पक्ष के आई पी कोर एकीकरण, परीक्षण, वितरण और उपग्रह डेटा प्रसंस्करण और मूल्य संवर्धन के लिए वस्तुओं की स्थापना शामिल है।

उद्देश्य और आवश्यकता का दायरा, निर्देशों के साथ सुपुर्दगी (deliverables) की सूची से युक्त संक्षिप्त "रुचि की अभिव्यक्ति" [EOI] , सक्षम विक्रेताओं को उनके प्रस्ताव तैयार करने में सहायता करने के लिए संलग्न है। पर्याप्त जानकारी, अनुभव और वित्तीय पृष्ठभूमि रखने वाले इच्छुक विक्रेताओं को हमारे "रुचि की अभिव्यक्ति" [EOI] आमंत्रण के अनुसार दस्तावेज़ जमा करके अपनी रुचि व्यक्त करने के लिए आमंत्रित किया जाता है।

सभी आवश्यक अपेक्षित जानकारी के साथ एवम जैसा कि "रुचि की अभिव्यक्ति" [EOI] दस्तावेज़ में विस्तृत है, "रुचि की अभिव्यक्ति" नीचे हस्ताक्षरकर्ता के पास , संदर्भ संख्या EOI/AOEP/2025/07-2-25/शुद्धिपत्र का उल्लेख करते हुए दिनांक 28-02-2025 को 14.00 बजे या उससे पहले पहुँच जानी चाहिए। तकनीकी विवरण, पिछला अनुभव, बुनियादी ढाँचा, वित्तीय मजबूती आदि। "रुचि की अभिव्यक्ति" [EOI] दस्तावेज़ ,अधिकृत हस्ताक्षरकर्ता द्वारा विधिवत भरे जाने चाहिए और "रुचि की अभिव्यक्ति" [EOI] के साथ संलग्न किए जाने चाहिए। अपर्याप्त/अपूर्ण जानकारी वाले "रुचि की अभिव्यक्ति" [EOI] को अस्वीकार कर दिया जाएगा। उन्नत आंकडा संसाधन अनुसंधान संस्थान (ADRIN) बिना कोई कारण बताए सभी या किसी भी ऐसी "रुचि की अभिव्यक्ति" को स्वीकार या अस्वीकार करने का अधिकार सुरक्षित रखता है। पात्रता मानदंडों को पूरा करके "रुचि की अभिव्यक्ति" [EOI] में भाग लेने वाले विक्रेताओं पर ही, अंतरिक्ष विभाग खरीद प्रक्रिया , का विधिवत पालन करते हुए विचार किया जाएगा।

वरिष्ठ क्रय एवं भण्डार अधिकारी

वरिष्ठ क्रय एवं भंडार अधिकारी
ईमेल– srpo@adrin.res.in
फ़ोन – 040 27781301

संलग्न: ईओआई एओईपी दस्तावेज़

भारत सरकार
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सत्यमेव जयते

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No: EOI/AOEP/2025/07-2-25/CORRIGENDUM

February 21th 2025

Dear Sir,

Invitation for "Expression of Interest" [EOI] for ADRIN Onboard Embedded Package (AOEP).

Advanced Data Processing Research Institute (ADRIN) under Department of Space, Government of India, is planning to develop a AOEP.

The development of AOEP Board includes design of hardware, software, firmware, board fabrication, third party IP core integration, testing, delivery and installation of the items for satellite data processing and value addition as mentioned in our EOI invitation

The brief EOI consisting of Objectives and Scope of requirement, List of deliverables with instructions is attached herewith to assist the competent Vendors to prepare their proposals. Interested Vendors having adequate know-how, experience and financial background are invited to express their interest by submitting the documents as per our EOI invitation.

"Expression of Interest" with all the necessary required information and as detailed in the EOI Document, shall reach the undersigned, quoting Reference No. EOI/AOEP/2025/07-2-25/ CORRIGENDUM on or before 14.00 Hrs, dated 28-02-2025. Technical details, Past Experience, Infrastructure, Financial Strength etc. EOI documents shall be duly filled by authorized signatory and attach along with EOI. Inadequate/incomplete information shall subject to rejection of EOI. ADRIN reserves the right to accept or reject all or any such "Expression of Interest", without assigning any reason whatsoever.

Vendors participated in the EOI by fulfilling the eligibility criteria only will be considered duly following the DOS Purchase Procedure.

Sr. Purchase & Stores Officer
Email – srpo@adrin.res.in
Phone – 040 27781301

Encl: EOI AOEP Document

INVITATION OF BIDS

EXPRESSION OF INTEREST (EOI)

FOR

DESIGN, DEVELOPMENT, INTEGRATION, TESTING AND DELIVERY OF

ADRIN ONBOARD EMBEDDED PACKAGE (AOEP)

ADVANCED DATA PROCESSING RESEARCH INSTITUTE(ADRIN)

DEPARTMENT OF SPACE

SECUNDERABAD–500009

1. OBJECTIVE

ADRIN, through this EoI, aims to select the vendor for the design, development, integration, testing and delivery of the AOEP for space applications as a turnkey solution. The broad objectives of the EoI are as defined here under: -

1. Design, Development, Integration, Installation, Testing and delivery of the AOEP as per the technical specifications and QA guidelines (Turnkey solution).

2. Testing of the hardware as per the model philosophy and test plan.

3. Delivery of all the hardware complete with interfacing, test jigs and documentations (including all design and analysis related documents& test reports).

4. Installation, integration and provision of technical support at the user specified site(s) and/or facilities.

5. Provision of necessary onsite training and warranty support.

The manufacturing of the mechanical housing, connecting harnesses, bare PCB etc. can be outsourced. However, the vendor shall indicate the subcontractors identified for carrying out the any of outsourced works in their response to this EoI.

2. General TERMS and CONDITIONS:

1. The tender is a two-part tender with technical evaluation followed by commercial evaluation. All the vendors shall submit their offers in two parts, i.e. Technical and Commercial bids **separately**.

2. The lowest offer from the technically qualified vendors shall be arrived at by considering all the cost elements of the items as specified in the list of deliverables.

3. The vendor shall complete the work according to the design, review and delivery milestones. The payment shall be released in consistence with the review and delivery milestones as indicated in the **Table 1.**

4. **All the design and development related activities including layout design, component procurement, reliability analyses, testing and evaluation, QA/QC activities and all other activities shall be carried out by vendor.**

5. The vendor may opt to subcontract manufacturing works like bare PCB fabrication, mechanical hardware fabrication, anodization etc. However complete item-wise list of such works shall be submitted in the technical bid.

6. Technical qualification of vendor has to be done strictly based on Vendor selection criteria given in **Table 2.**

7. Once assigned, the work specified is to be executed in complete, and no partial execution of work will be considered.

8. In case the vendor decides to exit without complete execution of work , the same will be considered as no work executed and any payment made till date will be refunded by the vendor to the Purchaser. In such case, ADRIN will return any delivered item to the vendor and penalty will be applied as per DOS purchase procedures.

9. The vendor shall provide a detailed technical compliance statement for offered products, specifications, guidelines and terms specified in the EoI.

10. Obsolete and outdated technology-based products shall not be quoted/offered.

11. Full technical specifications and literature must be provided for all the quoted items including sub-items to substantiate the compliance.

12. The fabrication & test facilities, manpower and the QA/QC processes/procedures in the vendor facilities must be certified by ISRO/DOS as per the applicable standards.

13. All standard and optional items, if any, must be clearly indicated in the list of deliverables.

14. The licensing information for software/hardware must be provided in detail wherever applicable.

15. The vendor shall furnish complete, reliably operating and secure systems. Design and selection of component and software shall be consistent with the requirements of long-term trouble-free operation with highest degree of reliability and maintainability.

16. Besides these, the vendor shall provide all necessary documents as per requirements.

17. Some of the specifications/interfaces are tentative and the same will be finalized during the PDR

18. The concept and the Design & Development of AOEP is the property of ADRIN and technically qualified lowest bidder has to sign NDA.

19. Vendor will be responsible to meet the delivery schedule indicated in the Table 1 and completion of all the design reviews such as MRR, PDR, CDR, TRR etc. indicated therein.

20. Vendor should agree for third party inspection in case it is required as per the QA.

21. All the Intellectual Property Rights (IPR) for the entire solution are reserved with ADRIN and Non-Disclosure Agreement (NDA) must be signed between ADRIN and vendor immediately after Purchase order acceptance.

22. Vendor should provide detailed breakup of the BOM submitting the bids.

23. **Delivery, Installation &Commissioning**:

    i. Vendor shall provide the installation, integration and support at **Hyderabad and Bengaluru.**
    ii. The supply of deliverables at the respective sites (Bengaluru and Hyderabad) will be informed in due course of time after award of the contract.
    iii. The vendor shall undertake to repair/replace the damaged/deficient items, maintaining the delivery schedule.
    iv. The vendor shall provide technical support and shall also be responsible for deputing qualified personnel for installation, testing, commissioning and other services under the Scope of Work.
    v. Mutually acceptable acceptance test procedure (ATP) document shall be

provided by the vendor.

vi. Acceptance Test on the supplied equipment must be conducted as per the ATP document.

24. The installation, commissioning and acceptance testing shall be completed within the mentioned timelines after supply of items.

25. Pre-Bid is mandatory. Offers of Vendors who attend Pre-Bid meeting will only be considered for evaluation. Otherwise offers will be rejected.

26. On-site Warranty support:

i. The warranty period for the Engineering Models and test jig boards along with associated Interface IP cores, wrapper logic shall be provided for a period of 3 years from the date of installation and acceptance.

ii. The warranty period for the space qualified boards shall be provided by the vendor for a period of 1 year from the date of installation and acceptance.

iii. The warranty shall also cover:

- All software/firmware upgrades/updates.

27. Details of training

Training schedule: Onsite training for porting and testing of ADRIN AOEP/IP cores with the top module/interfaces supplied by the vendor along with necessary documentation/media. Maximum of 10 Engineers.

28. Delivery and payment schedule:

Table 1 Delivery & Payment Schedule

Timeline (Months)	Activity	Payment	Remarks
T0	PO release date	30% of PO value excluding taxes as advance amount against BG.	---
T0 + 2	PDR	Not a payment milestone	
T0 + 5	MRR	Not a payment milestone	
T0 + 6	TRR	Not a payment milestone	
T0 + 8	AOEP (EM) and PSM (EM) with Test Jigs to be delivered.	Cost of Supplied Items +Taxes against BG	Payment will be released after acceptance of all the items.
T0 + 10	CDR	Not a payment milestone	
T0 + 15	AOEP (QM) and PSM (QM) delivery, qualification and completion.	Cost of Supplied Items +Taxes against BG	Payment will be released after acceptance of all the items.

T0 + 18	All AOEP (FM) and PSM (FM) delivery, integration, testing, simulation and installation	Balance Amount + Taxes & BG given prior to this milestone will be released by holding 10% as PBG towards warranty.	Payment will be released after acceptance of all the items.

Note:

1. **Clearance from User end is mandatory for proceeding to the next stage (as per Table1 and RFP).**
2. **LD clause applies, in case of Non-Compliance to the above schedule (Table1) from Vendor End.**
3. **Any delay in above Schedule (Table1) from End User during Technical Qualification of Deliverables due to Unforeseen Conditions, LD clause will not apply.**
4. **Number of Iterations required (if any) as per Table 1 towards Technical Compliance and Deliverables (as per RFP) to be taken care by the Vendor w.r.t. cost and time for meeting the delivery schedule (Table1), without any additional cost from End User.**

3. Vendor Evaluation Criteria

Industry Partner should have capability in terms of fabrication facility, storage facility development and test facility as well as necessary technical expertise to build, optimize, test and deliver the highly reliable space-grade products. Compliance Table 2 for Industry Partner's Capability Required for Realization of AOEP System with PSM for Space is given below. Requisite proof of compliance to be provided against each point, failing to provide proofs will be considered as non-compliance. The term Vendor in Compliance means Vendor and any of its sub-contractors (if any) engaged for execution of work as stated in EoI.

Table 2: Compliance

S. No	Capability	Vendor Compliance/submission requirements	Compliance
1.	EXPERIENCE: The vendor should have the following technical capabilities.		
1.1	Have credible history in Indigenous/In-House development and delivery of space borne sub-systems for ISRO spacecraft main-frame/payload systems for last five years.	Proof of delivery and acceptance to be submitted.	
1.2	Have demonstrated the in-house capability to design, develop, qualify and deliver space-borne mainframe/ payload sub-systems consisting of space grade components with space qualified personnel and infrastructure.	Proof of certified personnel and infrastructure to be submitted.	
1.3	Have developed and space qualified Onboard mainframe/payload systems, Power Supply Modules for Space craft subsystems.	ATP reports to be submitted as proof incase it's not sensitive.	
1.4	Have the credentials of procuring space components with necessary procurement specifications, storage and documentation	. Previous purchase orders, details of storage facility for components to be submitted.	
1.5	Have the experience and in-house infrastructure for up screening of components for Space applications.	Proof of infrastructure facility installation and previous up screened components details to be submitted.	
1.6	Expertise in High-Speed(>2GHz) Digital Board Design for Space based mainframe/payload designs.	Previous Supply Order and associated Block Diagram depicting the ICs /components used in design to be submitted as proof incase it's not sensitive.	
1.7	Have credentials in designing Controller cards based on Microchip FPGA for Space based mainframe/payload application	. Previous Supply Order and associated Block Diagram depicting the above ICs/components to be submitted as proof incase it's not sensitive.	

1.8	Have credentials in designing digital sub-systems based on Space grade FPGAs.	Previous Supply Order and associated Block Diagram depicting the above ICs/components to be submitted as proof incase it's not sensitive.	
1.9	Have the expertise to implement the algorithms in FPGAs for Space based payload application.	Previous Supply Order and associated Block Diagram depicting the above ICs/components to be submitted as proof incase it's not sensitive.	
1.10	Have credentials in designing digital sub-systems based on High-Speed>2GHz) space grade SerDes transceivers.	Previous Supply Order and associated Block Diagram depicting the above ICs/components to be submitted as proof incase it's not sensitive.	
1.11	Have design credentials as a Qualified source for mounting Space grade CQFP implemented on a PCB.	Proof of delivery and acceptance to be submitted.	
1.12	Have credentials in Qualified processes for CQFP assembly on Multi-layer boards.	Proof of delivery and acceptance to be submitted.	
1.13	Have credentials in achieving Thermal Performance through Multi-layer boards with high power (~25W) for Space based payload value addition.	Proof of delivery and acceptance to be submitted.	
1.14	Have the expertise to assemble the complex digital board in-house at the approved line and with space certified personnel.	Proof of delivery and acceptance to be submitted.	
1.15	Qualified source for Hybrid Micro Circuits (HMC) for development of Power Supply Modules.	Proof of delivery and acceptance to be submitted.	
1.16	Have the expertise for designing and qualifying High Wattage (>25W) PSMs for Space based payload application.	Proof of delivery and acceptance to be submitted.	
1.17	Have the expertise to develop Test Jigs which will act as the Baseband Data Handler (BDH) simulator for simulating Payload data interfaces and Onboard	Proof of delivery and acceptance to be submitted if available in the similar area.	

	Computer (OBC) simulator for simulating data/command interfaces and can be integrated to the Space based AOEP system during testing.		
1.18	Vendor should have an ESD safe laboratory for component mounting and fabrication, which can be inspected.	Compliance mandatory	
1.19	Organization should have experience in designing for EMI-EMC.	Proof of delivery and acceptance to be submitted.	
1.20	Organization should have experience in designing for Thermal specification.	Proof of delivery and acceptance to be submitted.	
1.21	Experience in FPGA logic design for Manchester encoding and decoding.	Proof of delivery and acceptance to be submitted.	
1.22	Experience in NOR Flash and SRAM memory interface design directly from FPGA, without any processor/ Microcontroller.	Proof of delivery and acceptance to be submitted	
1.23	Experience in differential/single ended FPGA designs.	Proof of delivery and acceptance to be submitted	
1.24	Vendor should ensure that FPGA controller digital cards meet the electrical constraints such as voltage and current supply, drive capabilities, external load, rise time and fall time.	Proof of delivery and acceptance to be submitted.	
2.	**MANPOWER:**		
2.1	The vendor should have dedicated and adequate certified trained manpower (at least 15 personnel) to carry out Electronic & Mechanical Fabrication for Space based systems.	Proof of certified personnel to be submitted.	
2.2	The vendor should have the prior experience and domain specialists to perform tests to clear the interfaces between Space based sub systems.	Experience profile of specialists to be submitted as proof wherever possible.	
3.	**INFRASTRUCTURE:**		

3.1	The vendor should have in-house infrastructure required to take up development work (Built to Specs and Built to Design) for space applications as per SPACE qualified QA processes.	Proof to be submitted incase for third party facility.	
3.2	The vendor should have infrastructure/tools like Hyperlynx or Cadence Allegro or similar tools required to design and develop layout for Digital High-Speed boards.	Proof to be submitted	
4.	**FABRICATION:**		
4.1	The vendor should have the following Clean Room facilities for Assembly and Testing of Space systems as per Space standards. • Class 100K: for PCB assembly and testing. • Class 10K: for Microelectronics. • Class 100: for Laminar-flow.	Proof to be submitted	
4.2	The vendor should have Capability/ Tools/ Infrastructure for workmanship as per SPACE standard for fabrication of electronic packages and for qualifying the material and processes used in realizing the hardware as given below. • ISROPAX 300 for PCB Fabrication • ISROPAX 301 for PCB Design • ISROPAS 206 for Microelectronics • ISROPAS 201 and 100 for Quality system • ISROPAS400 for Clean room • IPC-2221 or ECSS-Q-ST-70-12Cfor PCB layout design rules. • IPC2152 or ECSS-Q-ST-70-12Cfor conductor width and spacing settings. • IPC7351 or ECSS-Q-ST-70-12C for foot print design of SMD components. • ISRO-PAX-301 or ECSS-Q-ST-70-	Proof to be submitted based on the previous experience to the extent possible.	

	12Cfor through hole devices.		
4.3	The vendor should have the ability and necessary tools for signal integrity and power integrity analysis as per space standards	Proof to be submitted	
4.4	The vendor should have in-house CAD facility for carrying out layouts compliant to space standards.	Proof to be submitted	
4.5	The vendor should have experience to follow SPACE QA guidelines for documenting, manufacturing, process flow chart to indicate critical process parameters, inspection checkpoints, instruments used in manufacturing these components including parameter setting etc. for all stages of fabrication, assembly and testing.	Proof to be submitted	
5.	**TEST FACILITY/EQUIPMENTS**		
	The vendor should have infrastructure for testing Digital Systems with test and measuring equipment like (Power Meter, Linear Power Supplies with digital voltage and current meters, Analog/Digital Multi Meters, Automatic data logging system, oscilloscopes and Other related Test Jigs/ATEs).	Proof to be submitted	
6.	**PROCUREMENT OF PARTS & MATERIALS**		
6.1	The vendor should have the experience to procure, qualify and facility to store the devices adhering to Space Standards as per the BOM, meeting the acceptance Quality Level and verification of quality (VOQ) from the Qualified Parts List (QPL).	Proof to be submitted	
6.2	The vendor must follow SPACE QA guidelines to procure devices from manufacturing lines with Space capability	Proof to be submitted	

	and select Manufacturer/Foundry based on fabrication & testing requirements.		
6.3	The vendor should have in-house infrastructure for screening Non- Qualified Materials/Components List.	Proof to be submitted	
7.	**RELIABILITY ASSURANCE INFRASTRUCTURE:**		
	The vendor should have Capability or access to Tools/Infrastructure in Reliability Engineering (e.g. Reliability Prediction, Failure mode Effect & Critical Analysis, Fault Tree Analysis, Life Test etc.) and Reliability Screening (e.g. to conduct Baking, Thermal Acceleration, Vibration, Leak Test as per SPACE QA standard.	Proof to be submitted	
8.	**ANALYSIS INFRASTRUCTURE:**		
	The vendor should have Capability or access to Tools/Infrastructure for carrying out Reliability analysis, worst case analysis, Thermal Analysis, De-rating/Stress Analysis, Structural Analysis, Junction Temperature Calculations, Experimental Verification of the temperature profile, Hot-spot identification, Thermal shunt designs and verification of its effectiveness as per SPACE QA standard.	Proof to be submitted	
9.	**QUALIFICATION TEST INFRASTRUCTURE:**		
	The vendor should have Capability or access to Tools/Infrastructure for conducting climatic, Thermovac, Acceleration, Vibration Frequency, Sine Vibration, Random Vibration as per SPACE standard.	Proof to be submitted	
10.	**MANAGEMENT:**		

	The vendor should have Quality Management System certification ISO 9001:2015 and AS9100 or equivalent, Quality Control System to realize Space systems.	Proof to be submitted	
11.	**FINANCIAL:**		
	The vendor should have required financial resources to execute the order (Annual turnover should be greater than Rs.100 crores for the last five consecutive years)	Proof to be submitted	

4. Technical Details

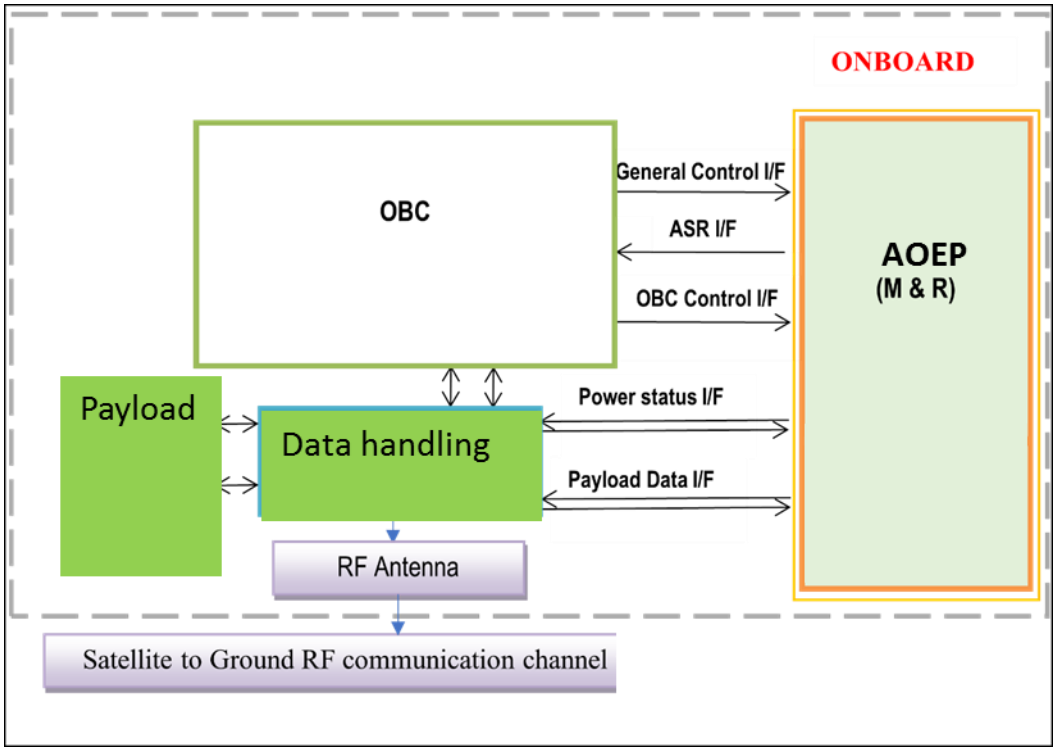

Figure 1: Typical Block diagram of AOEP.

ADRIN Onboard Package (AOEP) encompasses a comprehensive design that can handle value addition requirements for onboard Data Handling subsystem of the satellite. It consists of single stacked package – AOEP Main Card (M) and AOEP Redundan*t Card (R) in a single footprint. The Cards are also accompanied by their

respective Power supply modules (PSM) i.e., PSM Main (M) & PSM Redundant (R) and interfaced with onboard subsystems e.g. Data Handling and Onboard Computer (OBC). AOEP is empowered with Space Grade FPGAs (Field Programmable Gate Arrays) that serves as the primary compute element as well as all the required data and command interfaces. It performs value addition on digital data of payload subsystem and is optimized for required payload data rates and interfaces.

Figure 1 shows AOEP integrated with other onboard subsystems. AOEP has Data, Control and Data Command, Status and Power interfaces with the subsystems. AOEP performs value addition over data and is designed to be compatible with desired data rate and interface requirements of onboard data handling subsystem. Above all, in order to ensure its reliability and resilience in the harsh space environment, AOEP essentially needs to be equipped with space-qualified radiation-hardened components and radiation-tolerant circuitry.

5 MODEL PHILOSOPHY

The Implementation Methodology involves hardware development of AOEP system for space comprising of Engineering Model, Qualification Model and Flight Model. After functional verification using Engineering Model, go ahead will be given for the fabrication of the QM and FM. The design guidelines of space packaging and fabrication needs to be followed for all models. Development of all the models will be according to the Table 3 given below:

Table 3: Model Philosophy of AOEP& PSM

Sr.No.	FEATURES	Engineering Model (EM)	Qualification Model (QM)	Flight Model (FM)
1.	COMPONENTS/PARTS	Industrial Grade / MIL grade with Space grade component equivalent footprint (**OR**) Space Grade components only if Industrial grade not available with Space grade component equivalent footprint, with temp range: –15 to +60^{0}C (active)	Space Grade (QML V) only. In case of unavailability, MIL883(B) components to be up-screened to meet space qualification requirements	Space Grade (QML V) only. In case of unavailability, MIL883(B) components to be up-screened to meet space qualification requirements
2.	FABRICATION	PCBs, Connectors, form factor, Packaging etc. same	As per space qualified pcb norms	As per space qualified pcb norms

		as final flight hardware		
3.	MATERIALS	MIL Grade	Space Grade	Space Grade
4.	PROCESS	MIL Qualified	Space Qualified	Space Qualified

5.1 SCOPE OF WORK

This EoI document outlines the requirements for Design, Development and supply of AOEP for Space. Vendor is responsible for realization of AOEP, Integration, Testing and Performance Evaluation of AOEP for Space. The following items shall be developed & delivered by the vendor.

a. Engineering Models (**EM**) of AOEP and PSM along with Test Jigs
b. Qualification Models (**QM**) of AOEP and PSM
c. Flight Models (**FM**) of AOEP and PSM
d. AOEP IPCores/Wrapper Module (for all the interfaces with the scope of ADRIN_IP integration with Vendor Top Module)

In consistence with the development of the above-mentioned hardware and IP Core/Wrapper Module, the vendor shall carry out the works as mentioned hereunder. The following scope covers activities on a broad level.

a. Carry out design of AOEP and associated PSM as per the electrical and mechanical specifications. This includes completion of simulation of both the AOEP& PSM and generation of block schematics, circuit schematics, PCB layouts and Bill of Materials (BOM). **Detailed simulation results shall be provided w.r.t the applicable sections for which simulation has been performed. The vendor shall proceed further towards PCB layout and schematic design post concurrence of ADRIN on simulation results**

b. Development of the IP Cores/Wrappers for handling data, data commands and command control and other IPCores such as used for board functionality.

c. Development of source code of developed application software, HDL IP Cores, HDL interface glue/wrapper logic, HDL test bench, test jig software and test routines.

d. The vendor shall carry out the detailed reliability analysis including, but not restricted to, the structural analysis, thermal analysis, signal integrity analysis, derating and FMECA for both AOEP& PSM designs. The reliability analyses shall be

performed in accordance with the standard practices followed by ISRO as per the applicable guidelines.

e. The vendor shall generate the Interface Control Document (ICDs), all the reliability analysis reports, Process Identification Document (PID), QA/QC documents, detailed test plan and submit the same to the ADRIN for review. All the aforementioned documents shall be reviewed in the Preliminary Design Review (PDR)conducted by ADRIN/ISRO. Comprehensive list of required documents shall be communicated to the vendor at later stage post PO placement.

f. Vendor shall present circuit design, simulation results and the documents generated for the fabrication and testing of the AOEP& PSM and their test jigs along with the software code and IPCores/Wrappers developed in the Preliminary Design Review (PDR). The vendor shall proceed for mechanical box, bare PCB and EM fabrication in the indicated quantity only after successful PDR of detailed analyses, documents and codes by ADRIN/ISRO.

g. The vendor shall fabricate the EM of the AOEP and PSM by standards that are in conformance to the approved PID and BOM, develop the harnesses for interconnection and test jig.

h. It will be the vendor's responsibility to integrate the ADRIN's IP Core with the HDL wrappers and port and perform the functional verification on AOEP and handle all the interfaces.

i. All the tests on the EM shall be performed as per the approved test plan. The vendor shall submit the results of all the tests performed in accordance with the approved test plan and present the same during Comprehensive Design Review (CDR). ADRIN/ISRO shall review the test results and give clearance for the fabrication of QM& FM.

j. If any change in the hardware or software is found to be required during the review of EM results by ADRIN, the vendor will have to incorporate the suggested changes, with no implication on the delivery schedule of QM & FM. If changes are required in the bare PCB layout or mechanical box, it shall be the vendor's responsibility to carry out the required changes in same. In this case, the new approved layouts/designs only shall be used for QM and FM.

k. The vendor shall fabricate and test the AOEP& PSM QM as per the approved guidelines and documents and present the results in the subsequent reviews.

l. If any deviation or anomaly is observed in the CDR, the vendor will make necessary changes in the design or code and implement the same in the AOEP&

PSM QM &FMs. This shall have no implication on price and the delivery schedule of the hardware.

m. Post completion of the respective hardware as per the model philosophy, the vendor shall complete the delivery milestone of the hardware, documents and test jigs. The packaging and handling shall be done with due care and hardware shall be delivered in ESD packing with dust caps placed on the connectors of the AOEP/PSM and harnesses.

n. The documents shall be delivered in the hardcopy as well as the softcopy (CD/DVD) formats.

o. The necessary training and onsite installation, testing, commissioning and support shall be provided by the vendor.

5.2 DELIVERABLES

This section indicates the items to be delivered by the vendor. Both the documents and hardware as deliverables are detailed in the following sub-sections:

5.2.1 Hardware

The vendor shall deliver the hardware in quantities as shown in tables for each of the subsequent sections A through D.

AOEP& PSM package, test simulator and test jig should have "Fail-Safe" interfaces.

A. Engineering Model (EM)

Total FOUR (04) Nos. EM cards to be fabricated and integrated in THREE (03) EM Packages.

One EM Package to host two (02) EM cards stacked (Main & Redundant) along with two (02) Relay Cards (Main & Redundant) and two (02) PSM (Main & Redundant) respectively.

The remaining two EM packages will have one EM card, one Relay Card and one PSM each, respectively.

Table A: EM Deliverable

ITEMS	LIST OF ITEMS	QUANTITY	DESCRIPTION OF THE ITEMS
ITEM1	AOEP(EM) along with Test Jigs	4	This is the Engineering Model (EM) of AOEP.

ITEM2	PSM(EM)along with Test Jigs	4	Power Supply Modules required for powering up AOEP(EM) along with Test JIGs

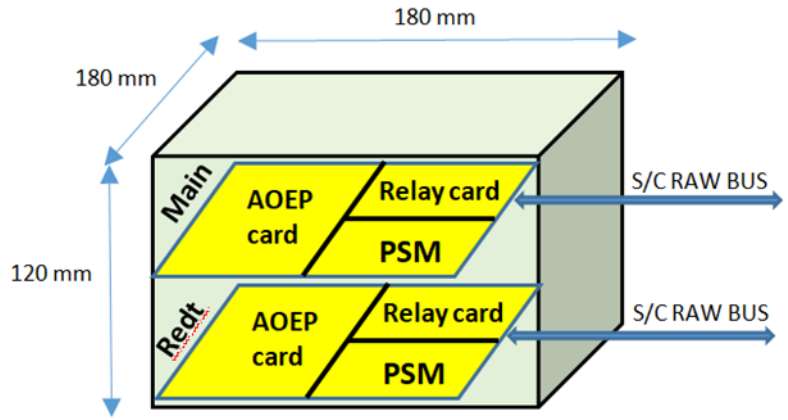

Figure 2

B. Qualification Model (QM)

Total ONE (01 No.) QM card to be fabricated and integrated in ONE (01) QM Package with equivalent dummy card (as redundant) in the Package Stack.

Table B: QM Deliverable

ITEMS	LIST OF ITEMS	QUANTITY	DESCRIPTION OF THE ITEMS
ITEM3	AOEP(QM)	1	This is the Qualification Model (QM) of AOEP
ITEM4	PSM(QM) PSM(QM)along with Relay card	1	Power Supply Modules required for powering up AOEP(QM)routed through Relay card

C. Flight Model (FM)

Total EIGHT (8 Nos.) FM cards to be fabricated and integrated in FOUR (04) FM Packages, with TWO (02) FM cards in each Package Stack (as in Figure 2)

Table C: FM Deliverable

ITEMS	LIST OF ITEMS	QUANTITY	DESCRIPTION OF THE ITEMS
ITEM5	AOEP(FM)	8	This is the Flight Model (FM) of AOEP.
ITEM6	PSM(FM)along with Relay card	8	Power Supply Modules required for powering up AOEP(FM)routed through Relay card

D. AOEP IPCores/Wrapper Module

Table D: AOEP IPCore/Wrapper Module Deliverable

S.NO.	LIST OF ITEMS	QUANTITY	DESCRIPTION OF THE ITEMS
ITEM7	AOEP IPCores/WrapperModule	1	This is the AOEP IPCores / Wrapper Top module that is required for handling all the interfaces of AOEP hardware. The Vendor has to identify, develop/procure and integrate the required IPCORES along with wrapper functions for development of full functionality of AOEP hardware along with the scope for ADRIN_IP

5.2.2 Documents

A. Monthly Progress report

B. Preliminary Design Review Document

C. Manufacturing Readiness Review Document

D. Comprehensive Design Review Document

E. Test Readiness Review Document

F. End Item Data Package (EIDP)

G. Test Reports, QA Clearance, Applicable Certification

The documents and contents listed above are indicative and exact nature and content of same or further additions shall be communicated post PO placement.