भारतसरकार / Government of India
अंतरिक्षविभाग / Department of Space
यू.आर. रावउपग्रहकेंद्र / U.R.RAO SATELLITE CENTRE
एच.ए.एल. एयरपोर्टरोड, विमानापुराडाक / HAL Airport Road, Vimanapura Post,
बेंगलूरु/ BENGALURU – 560 017

Ref No.: ISAD/2025-0-64331 19.06.2025

ऑनबोर्ड व भूस्टेशन उपयोग के लिए अंतःस्थापित डेटा संसाधन माड्यूल(ई डी पी एम) के लिए इच्छा की अभिव्यक्ति(ई ओ आई) के लिए आमंत्रण

Invitation for Expression of Interest [EoI] for Embedded Data Processing Module (EDPM) for onboard & ground station application

भारत सरकार के अंतरिक्ष विभाग के अंतर्गत भारतीय अंतरिक्ष अनुसंधान संगठन इसरो का यू आर राव उपग्रह केंद्र [यू आर एस सी] (जिसे पहले इसरो उपग्रह केंद्र के नाम से जाना जाता था), सभी भारतीय निर्मित उपग्रहों के डिजाइन, विकास, निर्माण तथा परीक्षण के लिए जिम्मेदार है। यू आर एस सी, वर्तमान में (ऑन बोर्ड व भू स्टेशन उपयोग के लिए अंतःस्थापित डेटा संसाधन माड्यूल (ई डी पी एम) के लिए अभिकल्प) हेतु उद्योग भागीदारों को आमंत्रण दे रहा है।

U.R. Rao Satellite Centre [URSC] (Formerly known as ISRO Satellite Centre), of Indian Space Research Organization [ISRO] under Department of Space, Government of India is responsible for Design, Development, Fabrication and Testing of all Indian made Satellites. URSC is currently inviting Industry Partners **for design of Embedded Data Processing Module (EDPM) for onboard & ground station application.**

उन भारतीय उद्योगों से इच्छा की अभिवयक्ति को आमंत्रित करने के लिए यह प्रस्ताव है जिनके पास ऑन बोर्ड व भू स्टेशन उपयोग हेतु अंतःस्थापित डेटा माड्यूल(ई डी पी एम) के अभिकल्प का कार्य करने की तकनीकी अवसंरचना तथा क्षमता है।

The proposal is to invite Expression of Interest exclusively from Indian industries having technical infrastructure and capability to execute **Design of Embedded Data Processing Module (EDPM) for onboard & ground station application**

यू आर एस सी उद्योग को आईएपी के लिए परीक्षण प्रणाली के आद्यंत विकास को स्वतंत्र रूप से करने में सक्षम बनाने तथा अंतरिक्ष यान से संबंधित गतिविधियों को करने के लिए निजी अंतरिक्ष उद्योगों में कुशल जनशक्ति विकसित करने के लिए स्थापना/रखरखाव और संचालन सहायता प्रदान करने में रुचि रखता है।

URSC is interested to enable the industry to carry out independently the end-to-end development of test system for IAP and provide the installation/maintenance and operation support to develop skilled manpower in the private space industries to carry out spacecraft related activities.

केवल उन भारतीय उद्योगों से इच्छा की अभिव्यक्ति को आमंत्रित करने का प्रस्ताव है जिनके पास आईएपी के लिए **परीक्षण प्रणाली के डिजाइन, विकास और कार्यान्वयन को निष्पादित करने तथा परियोजना गतिविधियों के दौरान परीक्षण प्रणाली गतिविधियों को सहायता प्रदान करने के लिए तकनीकी अवसंरचना और क्षमता है**

The proposal is to invite Expression of Interest exclusively from Indian industries having technical infrastructure and capability to execute **design, development and realisation of test system for IAP and support to the test system activities during project activities**

ई ओ आई दस्तावेज हमारे वेबसाइट www.isro.gov.in से डाउनलोड किए जा सकते हैं
EOI documents can be downloaded from our website www.isro.gov.in

ई ओ आई का मूल्यांकन बोलीदाताओं के अनुभव, सेवाओं के दायरे की उनकी समझ, सुविधा अवसंरचना, प्रस्तावित कार्यप्रणाली और कार्य योजना, कुशल जनशक्ति और उद्योग की वित्तीय ताकत के आधार पर किया जाएगा।

The EOI will be evaluated on the basis of bidder's experience, its understanding of scope of services, facility infrastructure, proposed methodology and work plan, skilled manpower and the financial strength of the industry.

यूआरएससी आवश्यकता पड़ने पर ईओआई की प्रक्रिया को रद्द/पुनः जारी करने या आगे की जानकारी/विवरण मांगने का अधिकार सुरक्षित रखता है।

URSC reserves the right to cancel/re-issue the process of EOI if the necessity so arises or to seek further information/details.

यदि कोई कंपनी/फर्म किसी भ्रष्ट या धोखाधड़ीपूर्ण व्यवहार में लिप्त पाई जाती है, तो उसे निविदा प्रक्रिया में भाग लेने से रोक दिया जाएगा और उसके ईओआई दस्तावेज़ पर विचार नहीं किया जाएगा।

Companies/Firms, if found to have indulged in any corrupt or fraudulent practices, will be debarred taking part in the Tendering process and their EOI Document will not be taken up for consideration.

इच्छा की अभिव्यक्ति के साथ-साथ आपूर्तिकर्ताओं/फर्मों को निम्नलिखित जानकारी भी विस्तार से प्रस्तुत करनी चाहिए:

Along with "Expression of Interest" Suppliers/ Firm[s]should furnish the following information also in detail:

1. कंपनियों का पंजीकृत पता के साथ, फोन, फैक्स, ईमेल, वेब आदि।
   Registered address of the Companies with Phone, Fax, Email, Web etc.
2. कंपनी/संगठन की स्थिति (स्वामित्व/साझेदारी/निजी/सार्वजनिक लिमिटेड आदि) के साथ मालिक, भागीदारों, निदेशक मंडल आदि के नाम और पता।
   Company/Organization Status (Proprietary/Partnership/Private/Public Ltd. etc.) with Name and Address of Proprietor, Partners, Board of Directors, etc.
3. सहयोगी: (ए) भारतीय (बी) विदेशी।
   Associates: (a) Indian (b) Foreign.
4. पिछले 3 वर्षों के दौरान प्रमुख ग्राहकों की सूची, पूर्ण पता और उनके संपर्क व्यक्ति।

List of Major Customers during the last 3 Years with full address and their Contact Persons.

5. स्वामित्व वाली/उपलब्ध अवसंरचना सुविधाओं का विवरण।
   Details of Infrastructure Facilities owned / available.
6. कंपनी के प्रमुख शेयरधारकों के नाम और पते तथा उनकी शेयर पूंजी का प्रतिशत।
   Names and addresses of the major Shareholders of the Company and the percentage of their share capital.
7. नवीनतम वार्षिक रिपोर्ट की प्रति के साथ पिछले 3 वित्तीय वर्षों के लिए पूंजी और कारोबार।
   Capital and Turnover for the preceding 3 Financial Years with copy of latest Annual Report.
8. उपलब्ध/वित्तीय क्षमता क्रेडिट सुविधाएं।
   Financial Capacity/Credit facilities available.
9. बैंकरों का नाम और पता।
   Name and Address of Bankers.
10. व्यापार संघ जिससे उद्योग/उद्योग जुड़े हुए हैं।
    Trade Association to which Industry/ies belong to.
11. संस्था/बिक्री/सेवा कर पंजीकरण संख्या।
    Establishment/Sales/Service Tax Registration Number.
12. व्यापार का प्रकार।
    Nature of Business
13. उनके बैंकरों द्वारा जारी फर्म की सॉल्वेंसी/वित्तीय क्षमता।
    Solvency/Financial capacity of the Firm issued by their Bankers.
14. उद्योगों की अन्य कोई प्रासंगिक जानकारियाँ हैं।
    Any other information the Industry/ies consider relevant.
15. सामर्थ्य और कमियों के क्षेत्रों को स्पष्टतः प्रकट करते हुए कंपनी/कंपनियों के प्रोफाइल
    The Profile of the Company/ies clearly bringing out the areas of Strength and Weaknesses.
16. ई ओ आई में भाग लेने के लिए तकनीकी और संगठनात्मक सामर्थ्य का स्व-मूल्यांकन।
    Self-Assessment Technical and Organizational Competence to take part in the EOI.
17. ई ओ आई में उल्लिखित प्रत्युत्तर प्रपत्र
    Response forms as mentioned in the EoI

<u>ईओआई प्रतिक्रिया को पूरा करना/Completion of the EOI Response:</u>

a. कंपनी/फर्म को ईओआई दस्तावेजों में सभी निर्देशों, नियमों और शर्तों, प्रपत्रों, आवश्यकताओं और अन्य सूचनाओं का सावधानीपूर्वक अध्ययन करने की सलाह दी जाती है। ईओआई प्रस्तुत करना ईओआई दस्तावेजों के सावधानीपूर्वक अध्ययन और जांच के बाद किया गया माना जाएगा, जिसमें इसके निहितार्थों की पूरी समझ हो।
   The Company/Firms are advised to study all the instructions; Terms and Conditions; Forms; Requirements and other information in the EOI documents carefully. The submission of EOI shall be deemed to have been done after a careful study and examination of the EOI documents with full understanding of its implications.

b. इस ई ओ आई का जवाब सभी मामलों में पूर्ण और संपूर्ण होना चाहिए। ई ओ आई दस्तावेज द्वारा आवश्यक सभी जानकारी प्रस्तुत करने में विफलता या ईओआई दस्तावेजों के हर पहलू के प्रति पर्याप्त रूप से उत्तरदायी न होने वाला प्रस्ताव प्रस्तुत करना कंपनी/फर्म के जोखिम पर होगा और इसके परिणामस्वरूप दस्तावेज को अस्वीकार किया जा सकता है।
The response to this EOI should be full and complete in all respect. Failure to furnish all the information required by the EOI document or submission of proposal not substantially responsive to the EOI documents to every aspect will be at the risk of the Company/Firms and may result in rejection of the document.

c. प्रस्तुत किए गए ईओआई के सभी पृष्ठों पर क्रमांक होना चाहिए और अधिकृत हस्ताक्षरकर्ता द्वारा हस्ताक्षरित होना चाहिए।
All the pages of the EOI submitted must be numbered and signed by the authorized signatory.

d. ई ओ आई के संबंध में प्रचार करना सख्त वर्जित है और एजेंसी द्वारा प्रस्तुत किए गए ऐसे प्रचार किए गए ईओआई को अस्वीकार किया जा सकता है।
Canvassing in connection with the EOI be strictly prohibited and such canvassed EOI submitted by the Agency are liable to be rejected.

उपरोक्त सभी जानकारी के साथ इच्छा की अभिव्यक्ति नीचे दिए गए पते पर, उपरोक्त संदर्भ संख्या का उल्लेख करते हुए, नियत तिथि और समय तक पहुंच जानी चाहिए।
"Expression of Interest" with all the above information shall reach the address given below, quoting the above Reference Number on or before the due date & time.

वरिष्ठ प्रधान, क्रय एवं भंडार/Sr. Head, Purchase & Stores
यू आर राव उपग्रह केंद्र/U R Rao Satellite Centre,
एचएएल एयरपोर्ट रोड/HAL Airport Road,
Vimanapura Post, Bengaluru/विमानपुरा पोस्ट, बेंगलुरु 560 017,
कर्नाटक, भारत/Karnataka, India

कृपया ईओआई संख्या का उल्लेख करते हुए अपने स्पष्टीकरण ई-मेल पर भेजें: pso_a@ursc.gov.in. प्री-ईओआई मीटिंग में भाग लेने के लिए अनुरोध 03.07.2025 16:00 IST को या उससे पहले यहाँ उल्लिखित ई-मेल पर पहुँच जाना चाहिए। हालाँकि, ईओआई (हार्डकॉपी) का जवाब केवल ऊपर उल्लिखित डाक पते पर भेजा जाएगा)। ईमेल और फैक्स कोटेशन स्वीकार्य नहीं हैं। नियत तिथि और समय के बाद प्राप्त कोटेशन स्वीकार्य नहीं हैं।

Please address your clarifications quoting the EOI number to E-mail: pso_a@ursc.gov.in. Request for participation in Pre-EoI meeting shall reach on or before 03.07.2025 16:00 @ Hrs IST to the Email mentioned herein. However, response to EOI (hardcopy) shall be sent to above mentioned postal address only). **E-mail & Fax quotations are not acceptable. Quotation received after due date & time are not acceptable.**

स्पष्टीकरण प्रस्तुत करने की अंतिम तिथि Last date of submission of clarification	:	**30.06.2025 16:00 Hrs IST.**
प्री-ईओआई बैठक (,सम्मेलन कक्ष, स्वगत कक्ष, यू आर एस सी में): Pre-EOI meeting (at Conference Hall, Reception, URSC)	:	**07.07.2025 10:00 Hrs IST.**
ईओआई प्रस्तुत करने की अंतिम तिथि Last date for submission of EOI	:	**07.08.2025 13:00 Hrs IST.**
ई ओ आई की खुलने की तिथि Opening date of EOI	:	**07.08.2025 14:00 Hrs IST.**

उपरोक्त सभी जानकारी के साथ इच्छा की अभिव्यक्ति **07.08.2025 @ 13:00 IST** बजे तक या उससे पहले उपरोक्त संदर्भ संख्या का उल्लेख करते हुए, नीचे हस्ताक्षरकर्ता तक पहुँच जानी चाहिए। यह प्रस्ताव पूर्व-ईओआई योग्यता के रूप में आरंभ किया गया है। यूआरएससी बिना कोई कारण बताए सभी या किसी भी इच्छा की अभिव्यक्ति को स्वीकार या अस्वीकार करने का अधिकार सुरक्षित रखता है।

"Expression of Interest" with all the above information shall reach the undersigned, Quoting above Reference Number on or before **07.08.2025 13:00 @ Hrs IST**. This proposal is initiated as a Pre-EOI Qualification. URSC reserves the right to accept or reject all or any such "Expression of Interest" without assigning any reasons what so ever.

-sd-

वरिष्ठ प्रधान, क्रय एवं भंडार

Sr. Head, Purchase & Stores

Expression of interest for design of Embedded Data Processing Module (EDPM) for onboard & ground station applications

Table of Contents

1. Introduction

U.R. Rao Satellite Centre (URSC) under Indian Space Research Organization (ISRO) is currently developing an Embedded Data Processing Module (EDPM) towards which the realization of associated space qualified electronics and mechanical design elements for on-board and equivalent high reliability electronics and mechanical design elements for ground station deployment is envisaged.

The development shall be carried out in two parts i.e., PART-A for ground station deployable hardware and PART-B for space flight qualified hardware. URSC is interested to engage an industry partner, with strong engineering and design background to be part of this development.

For both the development parts the selected vendor shall be responsible for design, development, realization, testing and delivery of two Engineering models (EM) and one Qualification Model (QM) of envisaged hardware. The vendor shall also be responsible to develop a common test-jig to test the hardware designed in both the parts and deliver two such test-jigs to URSC for validating the models.

The scope of this document is to provide the basic information related to EDPM and EOI process. It further specifies the detailed list of activities to be carried out along with terms & conditions for vendor selection.

1.1 Brief description of EDPM

The EDPM is a dedicated hardware platform realized to implement data processing algorithms used over satellite TM, TC and Payload data. The EDPM functionally can be sub-categorized to data processing and electronics power conditioning modules, the detailed specifications & requirements of which are mentioned in sections 3.2 & 3.3 for PART-A and 4.2 & 4.3 for PART-B

The EM shall be representative in form, fit and function to the final deployable design but realized using COTS equivalent parts. The EMs will be beneficial for carrying out functional

design validation, static & dynamic timing analysis, signal & power integrity analysis and EMI/EMC analysis which would act as feedback for validating and improving the final design.

The QM shall be equivalent to the final deployable design and is developed for final functional validation and full-level environmental tests. The QM shall have design updates post validation of EMs and specifically for PART-B it shall be subjected to flight package qualification campaign at vendor (or vendor leased) premises wherein it shall work reliably under launch vehicle vibration load test (tests include: random shock, low level sinusoidal and high level sinusoidal), EMI / EMC tests and thermal-vacuum variation test (tests include thermal cycling between -10^{o}C to +65^{o}C, hot soak at +65^{o}C & cold soak at -10^{o}C in 10^{-5} bar of pressure). The exact details of the tests included in the qualification campaign will be shared in the RFQ.

URSC invites your organization to submit a detailed proposal and proof of vendor expertise, as part of response for the EOI to develop engineering and qualification models of hardware unit and further mass manufacturing of prototype. Development activities for both parts involve hardware schematic design, layout design of PCBs, mechanical package design, PCB fabrication, component procurement, wiring, software required for board verification, development of test equipment, package assembly, testing, and realization of EMs and QM. **Subsequent to the completion of the development URSC shall hold complete rights to the product developed.**

2. EOI process and statement of work

2.1 EOI process

Expression of Interest (EOI) aims to identify a suitable vendor(s) for joint development of Embedded Data Processing Module (EDPM) and it will be a single stage process. A pre-bid meeting will be held to brief all the interested vendors regarding the process and complete plan. A detailed vendor selection criterion is provided in Section 5, **for which prospective vendors are required to provide all the documentary proofs as per the list**. All responses will be evaluated by a competent committee in URSC and a list of probable vendors capable of completing both the parts of the development will be selected.

The functional and technical specifications required to develop a proposal is provided in this EOI. Based on the data, vendor is expected to give an engineering proposal with all technical details adhering to standards mentioned in section 2.2.3.89 and 2.3.3.77 along with project execution plan. A presentation from vendor shall be sought to understand the proposal.

All received proposals will be evaluated based on the pre-defined criterion and list of selected vendors will be generated. An indenting process will be initiated in a *Limited tender mode* only on those vendors whose EOI is selected. A flow chart of the process is as shown in **Figure *1*** .**The final purchase order will be awarded to single or multiple parties (maximum two) to individually execute the order.**

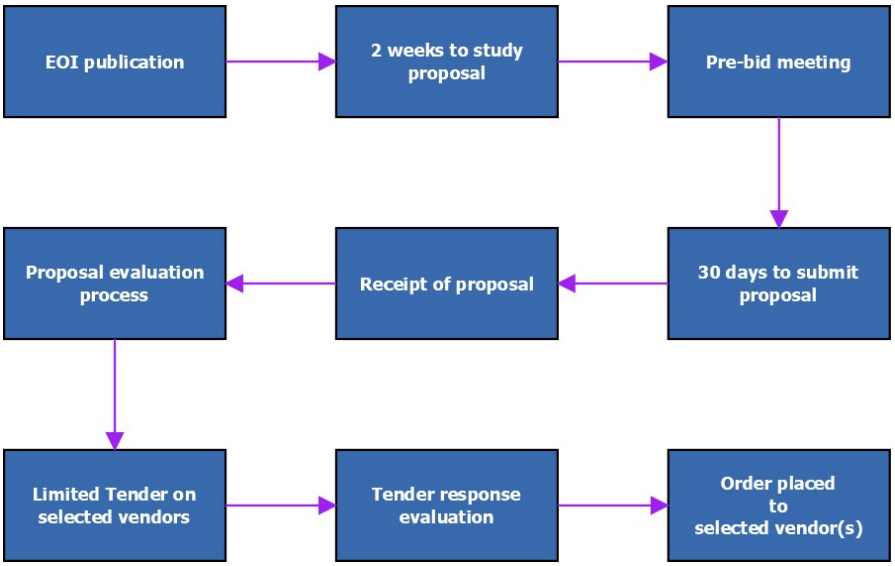

Figure 1. Flowchart of the EoI process

2.2 Statement of work for Part-A

This section provides a brief idea of the total work to be carried out by the vendor after receipt of order. The development cycle is divided into 3 phases

2.2.1 INITIAL PHASE

2.2.1.1. Initial phase starts after the PO is placed and Non-Disclosure Agreement (NDA) is signed between vendor and URSC.

2.2.1.2. Functional and technical specifications of the module in addition to that mentioned in EoI will be provided by URSC. Any suggestions or improvements can be proposed by vendor. Final decision to accept the proposal in part, total or to reject it is at URSC discretion.

2.2.1.3. Vendor needs to carry out

- 2.2.1.3.1. Schematic design
- 2.2.1.3.2. PCB design (electronics and mechanical) assessment
- 2.2.1.3.3. Assessment of expected PCB dimensions, choice of material for PCB, choice of material for mechanical housing
- 2.2.1.3.4. Mechanical design (both PCB level & package level)
- 2.2.1.3.5. Assessment and implementation of power and thermal management scheme

2.2.1.4. After design finalization by the vendor, a joint Preliminary Design Review (PDR) will be held by vendor to obtain clearance from URSC for continuing to next phases.

2.2.1.5. Following aspects shall be discussed at the PDR:

- 2.2.1.5.1. Schematic design review for hardware (reason and rationale)
- 2.2.1.5.2. Proposed BoM for both EM & QM
- 2.2.1.5.3. Rationale for arriving at a particular design mechanism / plan
- 2.2.1.5.4. Compliance to requirements specified in sections 3.3 & 4.3
- 2.2.1.5.5. Mechanical packaging and thermal management plan
- 2.2.1.5.6. EMI-EMC plan
- 2.2.1.5.7. Automated Test Equipment realisation plan
- 2.2.1.5.8. Test philosophy including qualification plan
- 2.2.1.5.9. Project execution plan and schedule
- 2.2.1.5.10. Process Identification Document (PID)

2.2.1.6. Depending on the lead-time criticality, vendor shall initiate the procurement of such components and material required adhering to quality standards mentioned in section 2.2.3.89 and 2.3.3.77 for the realization of EMs & QM.

2.2.1.7. They shall also initiate test jig / equipment fabrication which will be used for initial validation of EM & QM.

2.2.2 DESIGN PHASE

2.2.2.1. After initial phase clearance from URSC, the vendor shall initiate PCB layout with strict adherence to ISRO-PAX-301 later on followed by below mentioned analysis for electronics design.

2.2.2.1.1. Signal integrity analysis

2.2.2.1.2. Power integrity analysis

2.2.2.1.3. PCB and module thermal analysis

2.2.2.1.4. PCB and module structural analysis

2.2.2.2. Vendor shall initiate mechanical design and carry out package level structural & thermal analysis ensuring that they meet the required specifications.

2.2.2.3. After all the design objectives are met, vendor shall hold a joint Detailed Design Review (DDR) with URSC to obtain the clearance to proceed further.

2.2.2.4. DDR shall include review of the following activities

2.2.2.4.1. PCB design review

2.2.2.4.2. Final BoM

2.2.2.4.3. SI analysis report

2.2.2.4.4. PI analysis report

2.2.2.4.5. Thermal analysis report

2.2.2.4.6. Software requirements

2.2.2.4.7. Component procurement process

2.2.2.4.8. Fabrication process

2.2.2.4.9. Project plan and schedule

2.2.2.4.10. Test system adequacy

2.2.2.4.11. Test case coverage

2.2.2.4.12. PID

2.2.2.5. Subject to the functional clearance of first EM by URSC, "*INITIAL PHASE*" for PART-B shall be commenced by vendor.

2.2.2.6. DDR clearance from URSC is a mandatory requirement to continue further phases.

2.2.3 EM REALIZATION PHASE

2.2.3.1. Vendor shall carry out component procurement, PCB fabrication, mechanical housing fabrication, wiring of the cards, card level and package level testing at vendor's premises for initial clearance using vendor's testing equipment.

2.2.3.2. Vendor shall hold a joint EM test results review with URSC and obtain the clearance to proceed further.

2.2.3.3. Post adequate test clearance at vendor facility, the first realised EM along with test-jig shall be delivered to URSC for functional validation and additional testing.

2.2.3.4. URSC will ensure all the design specifications are met and shall bring out any design flaws, issues or improvements (if any) to be done for the subsequent EM.

2.2.3.5. Any issues observed during the first EM testing need to be reviewed, addressed and resolved before proceeding to fabrication of second EM and QM.

2.2.3.6. Delivery of second EM and QM with necessary corrective implementation as observed during first EM.

2.2.3.7. Failure of components during any phase of testing shall be reported to URSC for analysis.

2.2.3.8. Test results review shall include a review of the following activities

2.2.3.8.1. Fabrication reports review

2.2.3.8.2. Process review

2.2.3.8.3. Vendor side test results review

2.2.3.8.4. PID

2.2.3.9. The component selection criteria shall be as follows

2.2.3.9.1. For EM: COTS or industrial parts which are functional equivalent and with same PCB footprint to the parts proposed for QM

2.2.3.9.2. For QM: Components shall be rated for Industrial or Automotive or Mil-grade wherein the final design (hardware & software) must adhere to ISO61508 SIL 3 safety level and MIL-STD-461G for EMI / EMC conformance.

2.3 Statement of work for Part-B

The development cycle is divided into 3 phases same as with Part-A

2.3.1 INITIAL PHASE

2.3.1.1. Initial phase starts after the functional test clearance of first EM realised for PART-A.

2.3.1.2. Suggested BoM of major components, functional and technical specifications of the module in addition to that mentioned in EoI will be provided by URSC. Any suggestions or improvements can be proposed by vendor. Final decision to accept the proposal in part, total or to reject it is at URSC discretion.

2.3.1.3. Vendor needs to carry out

- 2.3.1.3.1. Schematic design
- 2.3.1.3.2. PCB design (electronics and mechanical) assessment
- 2.3.1.3.3. Assessment of expected PCB dimensions, choice of material for PCB, choice of material for mechanical housing
- 2.3.1.3.4. Mechanical design (both PCB level & package level)
- 2.3.1.3.5. Assessment and implementation of power and thermal management scheme

2.3.1.4. After design finalization by the vendor, a joint Preliminary Design Review (PDR) will be held by vendor to obtain clearance from URSC for continuing to next phases.

2.3.1.5. Following aspects shall be discussed at the PDR stage:

- 2.3.1.5.1. Schematic design review for hardware (reason and rationale)
- 2.3.1.5.2. Proposed BoM for both EM & QM
- 2.3.1.5.3. Rationale for arriving at a particular design mechanism / plan
- 2.3.1.5.4. Adherence to PCB Design rules / guidelines
- 2.3.1.5.5. Compliance to requirements specified in sections 3.3 & 4.3
- 2.3.1.5.6. Mechanical packaging and structural dynamics
- 2.3.1.5.7. Thermal management plan
- 2.3.1.5.8. EMI-EMC plan
- 2.3.1.5.9. Test system (Automated Test Equipment) realisation plan
- 2.3.1.5.10. Test philosophy including qualification plan
- 2.3.1.5.11. Project execution plan and schedule

2.3.1.5.12. PID

2.3.1.6. Depending on the lead-time criticality, vendor shall initiate the procurement of all the components / material required adhering to quality standards mentioned in section 2.2.3 for the realization of EMs & QM.

2.3.1.7. They shall also initiate test jig / equipment fabrication which will be used for initial validation of EM & QM.

2.3.2 DESIGN PHASE

2.3.2.1. After initial phase clearance from URSC, the vendor shall initiate PCB layout with strict adherence to ISRO-PAX-301 and followed by below mentioned analysis for electronics design.

2.3.2.1.1. Signal integrity analysis

2.3.2.1.2. Power integrity analysis

2.3.2.1.3. PCB and module thermal analysis

2.3.2.1.4. PCB and module structural analysis

2.3.2.2. Vendor shall initiate mechanical design and carry out package level structural & thermal analysis ensuring that they meet the required specifications.

2.3.2.3. After all the design objectives are met, vendor shall hold a joint Detailed Design Review (DDR) with URSC to obtain the clearance to proceed further.

2.3.2.4. DDR shall include review of the following activities

2.3.2.4.1. PCB design review

2.3.2.4.2. Final BoM

2.3.2.4.3. SI analysis report

2.3.2.4.4. PI analysis report

2.3.2.4.5. Thermal analysis report

2.3.2.4.6. Structural analysis report

2.3.2.4.7. Software requirements

2.3.2.4.8. Component procurement process

2.3.2.4.9. Fabrication process

2.3.2.4.10. Project plan and schedule

2.3.2.4.11. Test system adequacy

2.3.2.4.12. Test case coverage

2.3.2.4.13. PID

2.3.2.5. DDR clearance is a mandatory requirement to continue further phases

2.3.3 EM REALIZATION PHASE

2.3.3.1. Vendor shall carry out component procurement, PCB fabrication, mechanical housing fabrication, wiring of the cards, card level and package level testing at vendor's premises for initial clearance using vendor's testing equipment.

2.3.3.2. Vendor shall hold a joint EM test results review with URSC and obtain the clearance to proceed further.

2.3.3.3. Post adequate test clearance at vendor facility, the first realised EM along with test-jig shall be delivered to URSC for functional validation and additional testing. URSC will ensure all the design specifications are met and shall bring out any design flaws, issues and minor changes or improvements to be done for the subsequent EM.

2.3.3.4. Any issues observed during the first EM testing need to be reviewed, addressed and resolved before proceeding to fabrication of second EM and QM.

2.3.3.5. Delivery of second EM and QM with necessary corrective implementation as observed during first EM.

2.3.3.6. Test results review shall include a review of the following activities

2.3.3.6.1. Fabrication reports review

2.3.3.6.2. Process review

2.3.3.6.3. Vendor side test results review

2.3.3.6.4. PID

2.3.3.7. The component selection criteria shall be as follows

2.3.3.7.1. For EM: COTS or industrial parts which are functional equivalent and with same PCB footprint to the parts selected for QM

2.3.3.7.2. For QM (URSC shall suggest the major parts to be used)

- Digital, analog and power parts shall have the following radiation performance
  - Single-Event Latch-up (SEL) immunity to LET > 80 MeV.cm^2 / mg
  - Single Event Upset (SEU) to LET > 30 MeV. cm^2/ mg
  - RHA up to TID => 30 krad (Si)

- Passives (resistors, capacitors, fuses, diodes, inductors, connectors etc.,) shall be qualified either for MIL-PRF-55342, MIL-PRF-55182, MIL-PRF-55681, MIL-PRF-55365, MIL-PRF-39010, MIL-PRF-38534, MIL-DTL-24308 & MIL-PRF-19500 depending on availability. The failure rate option shall be selected as "space-level" and non-availability of the same shall be communicated with URSC for selection of appropriate alternate option
- The DCDC proposed shall adhere to MIL-STD-461 G for EMI / EMC compliance
- All components shall exceed the NASA driven outgassing requirements in ASTM E-495 of Total Mass Loss (TML) of less than 1.0% and a Collected Volatile Condensable Material (CVCM) of less than 0.1% where ever applicable

2.3.3.8. Failure of components during any phase of the project shall be reported to URSC for analysis.

2.4 Responsibility matrix for Part-A

Phase	S. No	Activity	ISRO responsibility	Vendor responsibility
Initial phase	1	Electrical Interface Data	Y	
	2	Mechanical envelope requirements	Y	
	3	Thermal specification at package interface	Y	
	4	ESD specification	Y	
	5	Grounding scheme post PO release	Y	
	6	ICD for non-standard interface & updated EID post PO release	Y	
	7	Schematic (includes netlist, max frequency of operation, expected voltage and current per net, differential pairs) in Cadence ORCAD compatible .dsn file format.		Y
	8	Schematic review and acceptance		Y
	9	Gate review at vendor level and ISRO level	Y	Y
Design phase	10	PCB layout design		Y
	11	Mechanical design, connector selection & mechanical drawing		Y
	12	All Analysis listed in design phase		Y
	13	Gate review at vendor level and ISRO level	Y	Y
Engineering model realisation Phase	14	Component procurement for EMs		Y
	15	Package fabrication (engineering model)		Y
	16	Board power-up, verification and validation all interfaces at maximum capacity. All internal nets have to be energised during testing.		Y
	17	Individual cards testing and clearance for package assembly at vendor premises	Y	Y
	18	Tested cards assembling as package, tested after assembly and delivery to ISRO along with one test-jig		Y
	19	Package level review for clearance of first EM	Y	Y
	20	Based on review findings, required design corrections implementation		Y
	21	Delta review for the implemented changes	Y	Y
	22	Delivery to ISRO of the tested and verified second EM and QM subsequent to implementing changes suggested from delta review (Testing and verification shall be at vendor premises). Test-jig updates (if any) shall be carried out at ISRO premises by vendor.		Y
	23	Package level review to clear for Part-A closure	Y	Y

2.5 Responsibility matrix for Part-B

Phase	S. No	Activity	ISRO responsibility	Vendor responsibility
Initial phase	1	Electrical Interface Data	Y	
	2	Suggested BoM (includes part number, quality of component, expected thermal dissipation for high dissipating components)	Y	
	3	Mechanical envelope requirement	Y	
	4	Stiffness, Quasi Static Load, Shock Level	Y	
	5	Vibration (Sine & Random) specification for the package	Y	
	6	Thermal specification at package interface	Y	
	7	Vacuum specification	Y	
	8	Outgassing (RML & CVCM) requirement	Y	
	9	ESD specification	Y	
	10	EMI EMC specification	Y	
	11	Grounding scheme post PO release	Y	
	12	ICD for non-standard interface & updated EID post PO release	Y	
	13	Schematic (includes component finalisation, netlist, max frequency of operation, expected voltage and current per net, differential pairs) in Cadence ORCAD compatible .dsn file format.		Y
	14	Schematic review and vendor acceptance		Y
	15	Gate review at vendor level and ISRO level	Y	Y
Design phase	16	PCB layout design		Y
	17	Mechanical design, connector selection & mechanical drawing		Y
	18	All Analysis listed in design phase		Y
	19	Gate review at vendor level and ISRO level	Y	Y
Engineering model realisation Phase	20	Component procurement for EMs		Y
	21	Package fabrication (engineering model)		Y
	22	Board power-up, verification and validation all interfaces at maximum capacity. All internal nets have to be energised during testing.		Y
	23	Individual cards testing and clearance for package assembly at vendor premises	Y	Y
	24	Tested cards assembling as package, tested after assembly and delivery to ISRO along with one test-jig		Y
	25	Package level review for clearance of first EM	Y	Y

Phase	S. No	Activity	ISRO responsibility	Vendor responsibility
	26	Based on review findings, required design corrections implementation		Y
	27	Delta review for the implemented changes	Y	Y
	28	Realisation of second EM and QM subsequent to changes along with delivery of second EM		Y
	29	Flight qualification campaign tests and validation using QM		Y
	30	Validation of test results and subsequent delivery of QM to URSC	Y	Y
	31	Package level review to clear for project closure	Y	Y

3. Function specification and requirements of EDPM for PART-A

3.1 Introduction

The Embedded Data Processing Module (EDPM) for Part-A is a dedicated hardware platform realized in an intrusion resistant and tamper evident enclosure, to implement data processing algorithms for protecting the satellite telecommand, telemetry and payload communication chains in real-time.

It provides a peer to peer (p2p) bi-directional communication channel with the satellite ground station computers via ethernet at data rates of 1Gbps & 10 Gbps and a management port for authorized users to update the internal configuration of EDPM. The functional block diagram of the implementation is shown in Figure 2.

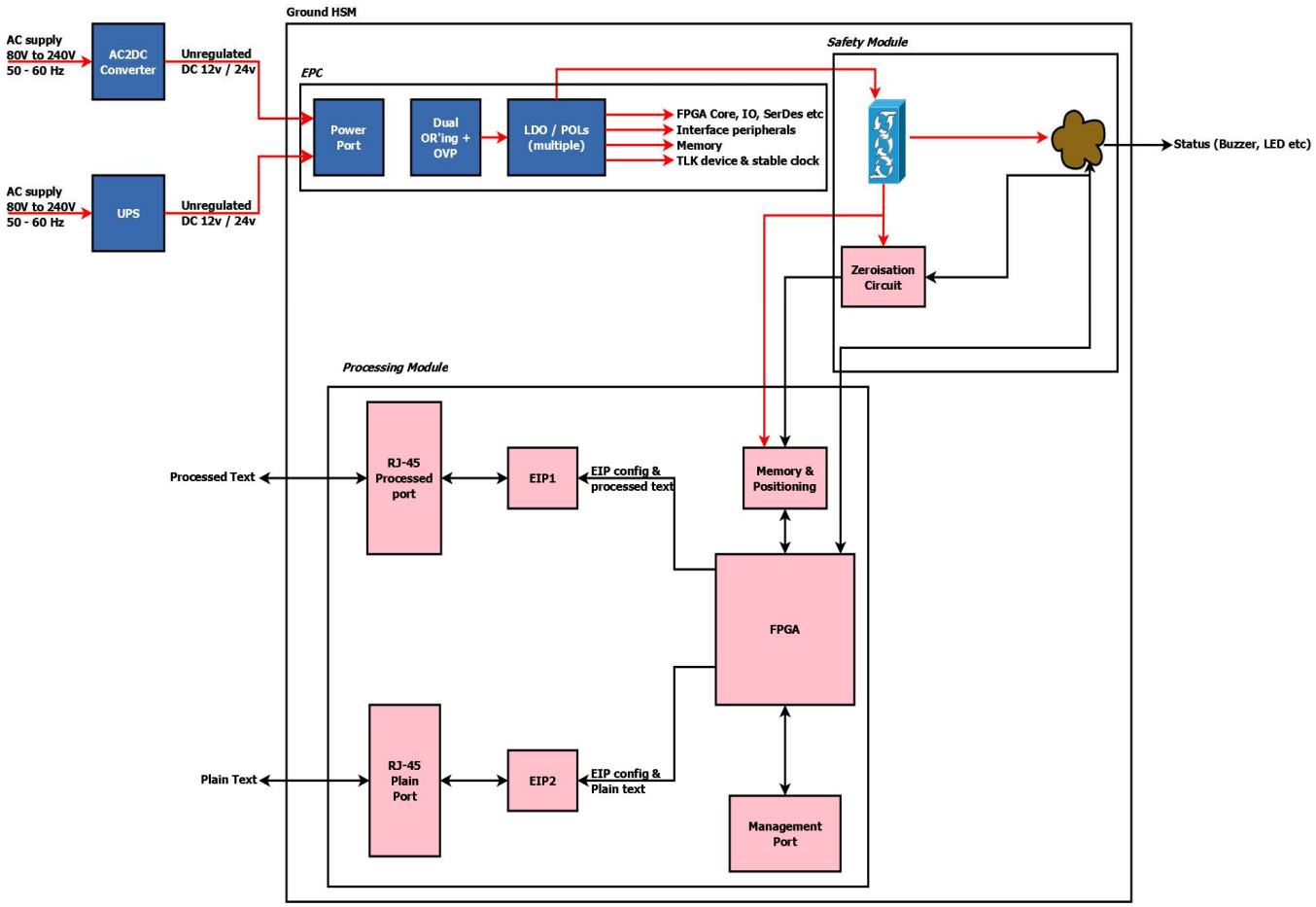

Figure 2 Functional block diagram of EDPM

3.2 Specifications

3.2.1 FUNCTIONAL SPECIFICATION OF DATA PROCESSING MODULE

The Data processing module shall be a hardware which provides the ability to implement data processing algorithms and peripheral interface logics on a FPGA connected to

3.2.1.1. Memory device(s) and positioning module: Used to store and access Design Programmable Parameters (DPPs) to aide data processing algorithms both onboard and ground along with keeping track of the deployed location.

3.2.1.2. Ethernet Interface peripheral 1: Provides access to receive DP data from the p2p connected ground station computer

3.2.1.3. Ethernet Interface peripheral 2: Provides access to transmit plain data from the p2p connected ground station computer

3.2.1.4. Management port peripheral: Provides access to reconfigure the DPPs and FPGA configuration

3.2.1.5. Zeroization circuit: Used for clearing the DPPs stored in memory devices when an intrusion is detected or when the energy storage element reaches a critical low energy state. This logic exists only for ground EDPM.

The components of Data processing module must derive its power from using an Electronics Power Conditioning (EPC) hardware housed inside the same enclosure.

3.2.2 FUNCTIONAL SPECIFICATION OF EPC

The EPC module shall be a hardware which realizes the required powering circuitry including voltage regulation and noise filtering along with implementing protection features like over-voltage protection, over-temperature protection and short circuit protection.

For the ground EDPM, the EPC shall also implement the safe charging and discharging circuitry needed for the energy storage element (battery, super capacitor etc.) which powers the intrusion detection mechanism and zeroization circuit for resetting / clearing the memory elements.

3.3 Requirements

3.3.1 TECHNICAL REQUIREMENTS

The following technical requirements shall apply to all hardware, software and firmware contained within the EDPM.

3.3.1.1. The ground EDPM shall be designed using components adhering to qualification mentioned in 2.2.3.89 with the following minimum specifications

3.3.1.1.1. FPGA: Shall be capable of supporting TCP / UDP / SNMP protocols and handling 1.0 / 10 G ethernet MAC signal rates with TSN protocols implemented in MAC. Logic elements: min. 140K LUTs and min. 120k DFF, Memory: min. 60 KB with EDAC and single bit error correction, min. operating frequency: 100 MHz, User IOs: min 250.

3.3.1.1.2. Memory & positioning module: Usable storage size after EDAC: 40 Mbit and a single supply dual band GNSS positioning module with integrated LNA.

3.3.1.1.3. Ethernet interface peripherals: Shall be capable of handling 1.0 / 10 G ethernet data rates with support for Time Sensitive Networking protocols (TSN).

3.3.1.1.4. Management port interface peripheral: Shall provide interface to access the FPGA and memory device for re-configuration.

3.3.1.1.5. Passives (resistor, capacitor, inductors, transformers, connectors etc.): Shall conform to standards mentioned in 2.2.3.89.

3.3.1.1.6. Energy storage element and circuitry: Design shall handle at-least 10 years of maintenance free lifecycle with provision to replace the energy storage element by authorised personnel

3.3.1.1.7. AC to DC power module: Shall conform to standards mentioned in 2.2.3.89 and support

- Input voltage support: 85 – 264 VAC, Single phase, 50 - 60 Hz
- Efficiency: 80% (min.)
- Load regulation of < 1%, isolation (input to output, input to case and output to case)
- Shall have auto recovery feature with short circuit protection, over-voltage protection and over-temperature shutdown

3.3.1.2. The EDPM shall have the following four logical interfaces ("input" and "output" are indicated from the perspective of the module)

3.3.1.2.1. DP port interface: All DP data that is to be processed by Data processing module i.e., processed telecommand, telemetry or payload data shall enter / exit via the "DP port" interface. This port shall be isolated in-case of triggering of tamper response circuit.

3.3.1.2.2. Plain port interface: All plain data that are counter-part to the DP data shall enter / exit via the "Plain port" interface.

3.3.1.2.3. Management port interface: All input commands, signals and control data used to control the operation of a Data processing module shall enter / exit via the "management port" interface.

3.3.1.2.4. Status output interface: All indicators, and status data such as physical indicators like buzzers, LEDs and displays used to indicate the status of EDPM shall exit via the "status output" interface. This interface is optional.

3.3.1.3. All external electrical power that is input to a data processing module (including power from an external power source or batteries) shall enter via a power port. The ground EDPM's power port must accept two power inputs (preferably IEC C16 port with latch) wherein the second will be connected during the scheduled maintenance of the regular line

3.3.1.4. The ground EDPM's enclosure shall be made intrusion resistant and tamper evident. It shall also implement tamper response mechanism like zeroization circuitry which would independently (without FPGA intervention) clear / reset the memory device content in the Data processing module to a known value.

3.3.1.5. The EDPM's EPC shall have an energy storage element and its associated recharging / discharging circuitry which works along with the zeroization circuit. This design shall perform the following function

3.3.1.5.1. Independently power the tamper response mechanism, zeroization circuit (and memory devices, in case of non-availability of AC power at power port). The minimum duration of supporting these logics must be twice the time taken for clearing / resetting the contents of the memory devices

3.3.1.5.2. Handle, isolate and report all failure conditions arising due to the energy storage element. Any failure must not affect the nominal functions of the Data processing module.

3.3.1.5.3. Initiate zeroization of memory device(s) in the following cases

- Nominal power through the power port is hindered
- Intrusion / tamper detection circuit is triggered
- FPGA request through management port

3.3.2 DOCUMENTATION REQUIREMENTS

The following documentation requirements shall apply to all hardware, software, and firmware contained within the EDPM.

3.3.2.1. Specify the hardware, software, and firmware components of EDPM, specify the data processing boundary surrounding these components, and describe the physical configuration of the module.

3.3.2.2. Specify the physical ports and logical interfaces and all defined input and output data paths of a data processing module.

3.3.2.3. Specify the manual (if any) or logical controls of EDPM, physical or logical status indicators, and applicable physical, logical, and electrical characteristics.

3.3.2.4. Contain a block diagram depicting all of the hardware components of Data processing module and component interconnections, including any input/output buffers, plain-text/DP-text buffers, control buffers, key storage, working memory, and program memory

3.3.2.5. Contain the design implementation pertaining to Built-in-self-test (BIST), Ethernet MAC, soft or hard macro-IP core (if any) and the bare-metal software code used (if any)

3.3.2.6. Contain the test-jig configuration, test vectors and the corresponding results for validation

3.3.3 VALIDATION REQUIREMENTS

The following design validation requirements shall apply to all hardware, software and firmware contained within the EDPM.

3.3.3.1. The Data processing module of both EDPM design shall be demonstrated by implementing multiple instances of open-source algorithms as suggested by ISRO in VHDL with the associated DPPs stored in memory device(s)

3.3.3.1.1. The first instance of algorithm processes data entering through plain port and this output processed data is asynchronously transmitted through DP port

3.3.3.1.2. The second instance of algorithm shall process and transmit (via plain port) sets of 256-byte demarcated data received every 0.512ms through DP port

3.3.3.2. The intrusion detection features incorporating requirements mentioned in section 3.3.1 shall be demonstrated

3.3.3.3. The EDPM must undergo a full-load burn-in test of 96 hours at room temperature

3.3.3.4. The effectiveness and proof of tamper evidence must be demonstrated

4. Function specification and requirements of EDPM for PART-B

4.1 Introduction

The Embedded Data Processing Module (EDPM) is a dedicated hardware platform realized in an intrusion resistant and tamper evident enclosure, to implement data processing algorithms for protecting the satellite telecommand, telemetry and payload communication chains in real-time.

It provides a peer to peer (p2p) bi-directional communication channel with the satellite

- On-Board Computer (OBC) via differential interface at data rates <256kbps
- Baseband Data Handling (BDH) system via SerDes interface at maximum supported line rate

and a management port for authorized users to update the internal configuration of EDPM.

The functional block diagram of the implementation is shown in Figure 3

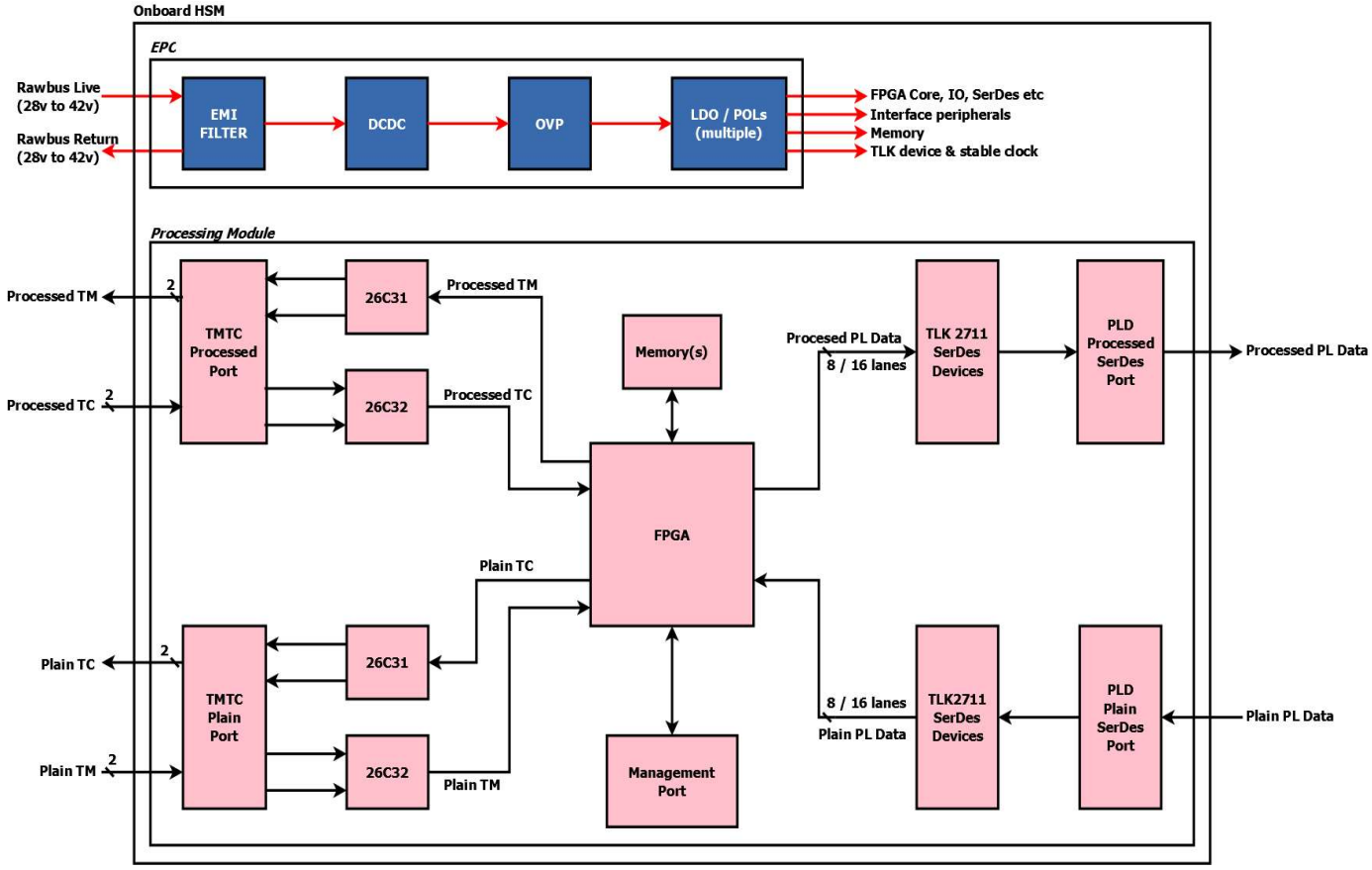

Figure 3. Functional block diagram of onboard EDPM

4.2 Specifications

4.2.1 FUNCTIONAL SPECIFICATION OF DATA PROCESSING MODULE

The Data processing module shall be a hardware which provides the ability to implement data processing algorithms and peripheral interface logics on a FPGA connected to

4.2.1.1. Memory device(s): Used to store and access Design Programmable Parameters (DPPs) to aide data processing algorithms both onboard and ground

4.2.1.2. Differential line drivers: Provides access to TMTC DP and plain text from OBC

4.2.1.3. TLK SerDes devices: Provides access to processed payload data from onboard BDH

4.2.1.4. Management port peripheral: Provides access to reconfigure the DPPs and FPGA configuration

The components of Data processing module must derive its power from using an Electronics Power Conditioning (EPC) hardware housed inside the same enclosure.

4.2.2 FUNCTIONAL SPECIFICATION OF EPC

The EPC module shall be a hardware which realizes the required powering circuitry including voltage regulation and noise filtering along with implementing protection features like over-voltage protection, over-temperature protection and short circuit protection.

4.3 Requirements

4.3.1 TECHNICAL REQUIREMENTS

The following technical requirements shall apply to all hardware, software and firmware contained within the EDPM.

4.3.1.1. The onboard EDPM shall be designed with the following mentioned components or components matching these minimum specifications

4.3.1.1.1. FPGA: RT4G150LCG1657V or equivalent

4.3.1.1.2. Memory: MYXREDPMS01GP32CL2-45/V-LGA142 or AS304GB32045nX0MBEY or equivalent

4.3.1.1.3. Differential line drivers: Radiation hard (refer 2.3.3.7) 26LVC31& 26LVC32 or equivalent

4.3.1.1.4. SerDes trans-receivers: TLK2711-SP or equivalent

4.3.1.1.5. EMI Filter & DCDC: Radiation hard (refer 2.3.3.77) with

- Operating input voltage between 26V and 48V
- Line regulation < 2% and load regulation < 10%
- Output ripple < 10% and Efficiency> 75% at half load

- Operating temperature range of -55°C to +85°C)
- Under-Voltage Lockout, Short Circuit, Output Over Voltage Limiter, Output Current Limiter and Overload Protection

4.3.1.1.6. LDO / PoL voltage regulators: Radiation hard (refer 2.3.3.77) and shall have soft-start, overcurrent protection, thermal shutdown and pre-bias startup (where applicable)

4.3.1.1.7. Passives (resistor, capacitor, inductors, transformers, connectors etc.): Shall conform to standards mentioned in 2.3.3.77.

4.3.1.2. The EDPM shall have the following logical interfaces ("input" and "output" are indicated from the perspective of the module)

4.3.1.2.1. DP port interface: All DP data that is to be processed by Data processing module i.e., processed telecommand, telemetry or payload data shall enter / exit via the "DP port" interface. This port shall be isolated in-case of triggering of tamper response circuit.

4.3.1.2.2. Plain port interface: All plain data that are counter-part to the DP data shall enter / exit via the "Plain port" interface.

4.3.1.3. All external electrical power that is input to a data processing module (including power from an external power source or batteries) shall enter via a power port.

4.3.1.4. The onboard EDPM's enclosure shall be "mechanically qualified" wherein its functional performance is assured during and after subjected to specified environmental level tests (dynamic and thermal excursions). Structural and Thermal environmental specifications for various tests will be shared post EoI and flight packages have to be qualified for these levels, and design compatibility of the developed engineering models with flight shall be demonstrated by analyses. The following sections expand upon the structural environmental test's requirement.

4.3.1.4.1. Dynamic test requirement

- Quasi Static Load: 30g (both in-plane & out of plane)
- Stiffness: >200 Hz first resonant frequency

4.3.1.4.2. Sine Vibration

Table 4.3.1.4.1: Sine Vibration Levels: Normal to Mounting Plane

Frequency (Hz)	Amplitude
	Qualification level
5 – 20	15.5 mm (0-p)
20 – 100	25 g
Sweep rate	2 oct. / min

Table 4.3.1.4.2: Sine Vibration Levels: Parallel to Mounting Plane

Frequency (Hz)	Amplitude
	Qualification level
5 – 20	15.5 mm (0-p)
20 – 100	25 g
Sweep rate	2 oct. / min

4.3.1.4.3. Random Vibration

Table 4.3.1.4.3: Normal/Parallel to Mounting Plane: Maximum Normal gRMS case

Frequency (Hz)	PSD (g^2 / Hz)
	Qualification level
20 – 100	+ 3 dB / oct
100 – 200	1.0
200 – 700	0.3
700 – 2000	- 6 dB / oct.
Overall g_{RMS}	18.4 g
Duration (Minutes)	2

4.3.1.4.4. Shock

Table 4.3.1.4.4: SRS Levels

Frequency (Hz)	SRS
100 – 1000	12 dB / oct.
1000 – 10000	2100 g

*Levels are for all 3 axes & Q=10

4.3.1.5. The mechanical volume of the design shall be contained in 150 cm x 150cm x 40cm with a weight less than 3Kg.

4.3.2 DOCUMENTATION REQUIREMENTS

The following documentation requirements shall apply to all hardware, software, and firmware contained within the EDPM.

4.3.2.1. Specify the hardware, software, and firmware components of EDPM, specify the data processing boundary surrounding these components, and describe the physical configuration of the module.

4.3.2.2. Specify the physical ports and logical interfaces and all defined input and output data paths of a data processing module.

4.3.2.3. Specify the manual (if any) or logical controls of EDPM, physical or logical status indicators, and applicable physical, logical, and electrical characteristics.

4.3.2.4. Contain a block diagram depicting all of the hardware components of Data processing module and component interconnections, including any input/output buffers, plain-text/DP-text buffers, control buffers, key storage, working memory, and program memory

4.3.2.5. Contain the design implementation pertaining to Built-in-self-test (BIST), Ethernet MAC, soft or hard macro-IP core (if any) and the bare-metal software code used (if any)

4.3.2.6. Contain the test-jig configuration, test vectors and the corresponding results for validation

4.3.3 VALIDATION REQUIREMENTS

The following design validation requirements shall apply to all hardware, software and firmware contained within the EDPM.

4.3.1.6. The Data processing module of both EDPM design shall be demonstrated by implementing multiple instances of open-source algorithms as suggested by ISRO in VHDL with the associated DPPs stored in memory device(s)

4.3.3.1.1. The first instance of algorithm processes data entering through plain port and this output processed data is asynchronously transmitted through DP port

4.3.3.1.2. The second instance of algorithm shall process and transmit (via plain port) sets of 256-byte demarcated data received every 0.512ms through DP port

5. Vendor selection

The vendor selection is a process to ensure that only organizations with the capability to carryout high-speed digital and mechanical designs to be part of the further process.

A detailed list of the vendor qualification criterion is provided in the Table 5.1 which needs to be provided by all the interested organizations. These responses will be evaluated by a committee in URSC and only those vendors who are able to provide all the data and proofs of meeting all the criterion only will be selected for further process.

Table 5.1: Vendor qualification criterion

Sl No	Criterion	Proof	Remarks
1	Experience in RTG4 or equivalent FPGA based board designs and board bring up.	Can provide a proof of similar FPGA experience from other manufacturers like Xilinx, Altera etc, but should be able to handle data rates from up to 12.5 Gbps.	Vendor shall demonstrate the product based on URSC request
2	Experience in working with 1G / 10G ethernet MAC with TSN and associated soft IP cores	--do--	--do--
3	Must have a static IP address for data sharing	Proof of IP allocation by registered ISP	-
4	Experience in design, development and maintaining an Automated test equipment for digital designs having interfaces with oscilloscopes, signal generators and network analysers.	Proof of designing the same for another client **OR** Any of the above requirement can be met by another entity with a letter of willingness to collaborate/support with the vendor.	Vendor shall demonstrate the product based on URSC request In-case of collaborating with another entity to meet this criterion, the vendor shall produce the partnering entity's proof of capability in form of a successfully completed PO of accomplishing the same
5	Experience in mechanical Package design qualified for aerospace standards.	Proof of previous purchase order **OR** Any of the above requirement can be met by another entity with a letter of willingness to collaborate / support with the vendor.	In-case of collaborating with another entity to meet this criterion, the vendor shall produce the partnering entity's proof of capability in form of a successfully completed PO of accomplishing the same

Sl No	Criterion	Proof	Remarks
6	Experience in PCB design with thermal handing capability > 10W over 2000 sq mm with continuous dissipation and implementing conduction cooled or conduction + radiation cooled environment.	Purchase order with a certification for successful completion **OR** Vendor should have a product present in the company catalogue /website meeting the requirement. **OR** Shall provide information on a product under development which can be demonstrated on demand	Vendor shall demonstrate the product based on URSC request
7	Experience in PCB fabrication and assembly with high pin count CCGA packages, Gigabit ethernet interfaces and high speed SERDES interface	Purchase order with a certification for successful completion **OR** Vendor should have a product present in the company catalogue /website meeting the requirement. **OR** Any of the above requirements can be met by another entity with a letter of willingness to collaborate/support with the vendor.	Vendor shall demonstrate the product based on URSC request In-case of collaborating with another entity to meet the criteria, the vendor shall produce requisite proof
8	Experience in package level testing of digital systems in a single package / card	--do--	--do--
9	Vendor should have an ESD safe laboratory (2KV rated) and of minimum space > 100 sq.m, which can be inspected. The said lab should have 24hrs CCTV surveillance with capability to record and store data continuously for minimum of 1 month. Surveillance data shall be made available to URSC as and when requested.	Compliance required.	
10	Experience in sourcing mechanical hardware / housing for electronic packages	Provide POs placed by the vendor on fabricators for material procurement, milling, anodising etc. **OR**	In-case of collaborating with another entity to meet this criterion, the vendor shall produce the partnering entity's proof of

Sl No	Criterion	Proof	Remarks
		Above requirement can be met by another entity with a letter of willingness to collaborate/support with the vendor.	capability in form of a successfully completed PO of accomplishing the same
11	Experience in performing the following analysis • Signal integrity (SI) analysis • Power integrity (PI) analysis PCB and package level thermal analysis conduction, conduction + radiation modes	Analysis reports carried out by the organisation internally on any package on card having frequencies greater than 10GHz (for SI, PI analysis), power dissipation greater than 15W in one PCB for thermal analysis with only conduction and radiative cooling. **OR** Any of the above requirement can be met by another entity with a letter of willingness to collaborate/support with the vendor.	Reports shall be attached along with the proposal In-case of collaborating with another entity to meet this criterion, the vendor shall produce the partnering entity's proof of capability in form of a successfully completed PO of accomplishing the same
12	Experience in sourcing EEE parts from OEM / authorised distributors with mandatory Certificate of Conformity (CoC) for every part used in the design	Provide POs placed by the vendor on OEM/distributor for components like FPGA, 32-bit microcontroller, memories etc **OR** Any of the above requirement can be met by another entity with a letter of willingness to collaborate / support with the vendor.	In-case of collaborating with another entity to meet the criteria, the vendor shall produce requisite proof
13	Organisation should have experience in designing electronics designs for a given thermal specification.	Purchase order with a certification for successful completion **OR** Vendor should have a product present in the company catalogue /website meeting the requirement. **OR** Any of the above requirement can be met by another entity with a letter	Reports shall be attached along with the proposal In-case of collaborating with another entity to meet this criterion, the vendor shall produce the partnering entity's proof of capability in form of a successfully completed PO of accomplishing the same

Sl No	Criterion	Proof	Remarks
		of willingness to collaborate/support with the vendor.	
14	Vendor shall have their own environment test facility or have access to a leasable recognised facility for performing thermovac, vibration / shock and EMI/EMC tests	Compliance required.	In-case of collaborating with another entity to meet the criteria, the vendor shall produce requisite proof
15	Vendor shall use a URSC or SAC qualified PCB fabrication line and PCB assembly (SMT) for the hardware realisation of PART-B's designs	Compliance required.	In-case of collaborating with another entity to meet this criterion, the vendor shall produce the partnering entity's proof of capability in form of a successfully completed PO of accomplishing the same
16	Vendor facility must be certified to ISO9001 series or AS9100 series or equivalent quality management & quality assurance standards	Compliance required.	
17	URSC requires all technical data to be shared by vendor for review and documentation. Work pertaining to schematic design, layout and PCB design has to be submitted to URSC in ORCAD™ compatible design files	Compliance required.	
18	Vendor shall sign a non-disclosure agreement with URSC after PO release.	Compliance required.	

6. EOI proposal

Vendor shall submit a brief EOI proposal including points listed in the table 6.1

Table 6.1 EOI proposal

Sl No.	Document name	Remarks
1	Organisation structure	
2	Project structure	This shall include roles and responsibilities.
3	Vendor Compliance	Compliance for vendor selection criterion and statement of work
4	Project plan	Shall contain the following • Work break-down structure • schedule for proto model • Gantt chart & critical path • suggestions to reduce the critical path
5	List of organisations	Details of organisations/companies who will be collaborating or vendor will be sub-contracting to, for various activities. Vendor should be responsible for final project and product outcome.
6	Detailed list of analysis	Following questions need to be addressed for each analysis • At what stage analysis will be done? • What is the success criterion? • Which software will be used? • Who will do?
7	PCB design (preliminary)	• Which standard will be used or what will be design rules? • Thermal extraction plan
8	PCB assembly plan	The document shall contain all details & process from PCB fabrication to conformal coating and potting.
9	Package concept drawing	
10	Thermal management plan	Preliminary analysis
11	Mechanical hardware fabrication plan	The document shall contain all the activities & process from material procurement to assembly with PCB.
12	Procurement plan for EEE parts	This document shall include for prototype • Supplier list • MOQ requirements • Lead times • Suggestion to handle lead times for prototype
13	List of software required	This document shall provide all the software required to carry out this activity. Software availability with organisation or procurement plan. In case of new software, training plan.
14	Risk analysis and mitigation plan	Clearly list out anticipated risks for each activity or design which can lead to delays and potential project slippages.
15	List of documents that will be shared with URSC at the end of Prototype	Clearly mention what each document will contain

7. Annexure 1: Abbreviations

ATE	Automated Test Equipment
BOM	Bill of Material
CVCM	Collected Volatile Condensable Materials
DPP	Design Programmable Parameter
DDR	Detailed Design Review
EDPM	Embedded Data Processing Module
EM	Engineering Model
EOI	Expression of Interest
EPC	Electronics Power Conditioning
FPGA	Field Programmable Gate Array
LED	Light Emitting Diode
MOQ	Minimum Order Quantity
PCB	Printed Circuit Board
PDR	Preliminary Design Review
PID	Process Identification Document
PI	Power Integrity
PO	Public Order
PoL	Point of Load power supplies
QM	Qualification Model
RML	Recovered Mass Loss
SI	Signal Integrity
TML	Total Mass Loss
URSC	UR Rao Satellite Centre