भारत सरकार/Government of India अंतरिक्ष विभाग/Department of Space यू.आर. राव उपग्रह केंद्र/U.R.RAO SATELLITE CENTRE एच.ए.एल एयरपोर्ट रोड, विमानपुरा पोस्ट, बेंगलूरु - 560017 HAL Airport Road, Vimanapura Post, BENGALURU – 560 017

Ref No. URSC/PUR/H/EOI/ISCP 2024062422

18.12.2024

<u>100 V बस के लिए IMPP की प्राप्ति हेतु इच्छा की अभिव्यक्ति का आमंत्रण (ईओआई)</u> Invitation for Expression of Interest [Eol] for the Realisation of IMPP for 100V BUS - reg

इसरो अगले पाँच वर्षों में अधिक संख्या में उपग्रहों को कक्षा में भेजने तथा प्रति वर्ष 15 से 20 उपग्रहों की प्राप्ति के मिशन पर अग्रसर है। इसके लिए अधिक संख्या के इलेक्ट्रॉनिक उप प्रणालियों के संविरचन, परीक्षण तथा समाकलन हेतु तैयार रखने की आवश्यकता है। उच्च-ऊर्जा उपग्रहों के बढती आवश्यकता को पूर्ण करने हेतु, 10-20 kW के आऊटपुट के हस्तन करने की क्षमता वाले एक ही ऊर्जा का उच्च वोल्टता ऊर्जा वाले बस की प्राप्ति की आवश्यकता पड़ती है। 1-6 k उपग्रह प्लेटफॉर्म हेतु एक उच्च वोल्टता (100V), उच्च ऊर्जा, माडूलर तथा इष्टतम ऊर्जा पैकेज की शुरुआत की गई है।

ISRO is embarking on a mission to produce large number of satellites to be put in orbit in the next five years and is all set to realize 15 to 20 spacecraft per year. This calls for a large number of electronic sub-systems to be fabricated, tested and made ready for integration. In order to meet the growing demand of high-power satellites, it becomes imperative to realise a high power & high voltage power bus capable of handling output power of 10-20 kW. A high voltage (100V), high power, modular and optimized power package for 1-6 k satellite platforms has been envisaged.

यू.आर.राव उपग्रह केंद्र (यू.आर.एस.सी), भारत निर्मित सभी उपग्रहों के अभिकल्प, विकास, संविरचन तथा परीक्षण हेतु भारत सरकार के अंतरिक्ष विभाग के तहत भारतीय अंतरिक्ष अनुसंधान संगठन(इसरो) का अग्रणी केंद्र है। वर्तमान में यू.आर.एस.सी. 100V बस के लिए समाकलित माडूलर ऊर्जा पैकेज (IMPP) का विकास कर रहा है।

U. R. Rao Satellite Centre [URSC], of Indian Space Research Organization [ISRO] under Department of Space, Government of India is the lead Centre of ISRO for Design, Development, Fabrication and Testing of all Indian made Satellites. Currently, URSC is developing integrated Modular Power Packages (IMPP) for 100V Bus.

100V बस के लिए समाकलित माडूलर ऊर्जा पैकेज (IMPP) की प्राप्ति हेतु इंजीनीयरिंग मॉडल (EM) के विकास हेतु इच्छा की अभिव्यक्ति का आमंत्रण का प्रस्ताव किया जाता है। पर्याप्त ज्ञान, अनुभव/सुविज्ञता तथा पर्याप्त वित्तीय पृष्ठभूमि वाले संभावित स्थापना/विक्रेता को उपरोक्त के लिए अपनी इच्छा की अभिव्यक्ति करने हेतु आमंत्रित किया जाता है।

It is proposed to invite Expression of Interest for development of Engineering Model (EM) hardware for realization of Integrated Modular Power Packages (IMPP) for 100V BUS. Potential Establishment[s]/ Vendor[s] having sufficient know-how, experience/expertise and sound financial background are invited to express their interest for the same.

ई ओ आई दस्तावेजों को हमारे वेबासाइट <u>www.isro.gov.in</u> से डाउनलोड किया जा सकता है।

EOI documents can be downloaded from our website www.isro.gov.in

ई ओ आई को बोलीकर्ता का अनुभव, सेवाओं के दायरे का ज्ञान, सुविधाओं की अवसंरचना, प्रस्तावित कार्य पद्धति तथा कार्य योजना, कुशल मानवशक्ति तथा उद्योग को वित्तीय सामर्थ्य के आधार पर मूल्यांकन किया जाएगा। साथ ही ई एम हार्डवेयर की सुपुर्दगी हेतु भारतीय उद्योग जिसमें सुदृढ इंजीनियरिंग, अभिकल्प तथा विश्लेषण पृष्ठभूमि है।

The EOI will be evaluated on the basis of bidder's experience, its understanding of scope of services, facility infrastructure, proposed methodology and work plan, skilled manpower and the financial strength of the industry. Also Indian Industry with strong engineering, design and analysis background for the delivery of EM Hardware.

क्रियाकलापों को अच्छी तरह समझने तथा कोई संदेह हो तो उसका निवारण करने हेतु यू.आर. राव उपग्रह केंद्र द्वारा एक पूर्व बोली बैठक का आयोजन किया जाएगा।

A Pre-EoI meeting will be arranged by U.R. Rao Satellite Centre, Bengaluru in order to have a better understanding of the activities involved, clarify doubts, if any.

यदि आवश्यकता हो तो ई ओ आई की प्रक्रिया को रद्द करने/पुनः जारी करने या आगे की सूचना/विवरण प्राप्त करने का अधिकार यू.आर.एस.सी. रखता है।

URSC reserves the right to cancel/re-issue the process of EOI if the necessity so arises or to seek further information / details.

यदि कंपनी/फर्म को किसी भ्रष्ट या कपटपूर्ण प्रथाओं में भाग लेने के बारे में ज्ञात हो तो उन्हें निविदा प्रस्तुत करने की प्रक्रिया से बहिष्कृत किया जाएगा और उनके ई.ओ.आई दस्तावेज पर विचार नहीं किया जाएगा।

Companies / Firms, if found to have indulged in any corrupt or fraudulent practices, will be debarred from taking part in the Tendering process and their EOI document will not be taken up for consideration.

तदुपरांत निम्नलिखित सूचना को विस्तार में इच्छा की अभिव्यक्ति के रूप में विक्रेताओं को प्रस्तुत करना होगा।

Subsequently, the vendor(s) shall submit the response to Expression of Interest along with the following information in detail:

1.	कंपनी का पंजीकत पते के साथ फोन फैक्स ईमेल बैव इत्यादि।
	Registered address of the company with Phone, Fax, Email, Web etc.
2.	कंपनी/संगठन की स्थिति (पी.एस.यू./स्वामित्व/एम.एस.एम.ई/भागीदारी/निजी लि./आदि) के साथ स्वामित्व भागीदार, बोर्ड के निदेशक का नाम व पता आदि।
	Company/Organization Status (PSU / Proprietary/MSME/ Partnership / Private
	Ltd., etc.) with Name and Address of Proprietor, Partners, Board of Directors etc.
3.	सहयोगीः (क)भारतीय (ख) विदेशीः व्यापार सह भागिता में प्रतिशत (यदि हो तो)
	Associates: (a) Indian (b) Foreign. Percentage of business partnership (if any).
4.	प्रमुख वर्तमान उपभोक्ताओं की सूची के साथ पूरा पता और उनके संपर्क ब्यौरे
	List of Major Current Customers with full address and their Contact/Details.
5.	अवसंरचना सुविधा का स्वामित्व/ उपलब्धता के ब्यौरे
	Details of Infrastructure Facilities owned / available.
6.	कंपनी के मुख्य भागीदारों के नाम व पता तथा उनके भाग की पूँजी का प्रतिशत।

	Names and addresses of the major shareholders of the Company and the
	percentage of their share capital.
7.	नवीनतम वार्षिक रिपोर्ट की प्रति सहित पिछले तीन वित्तीय वर्ष की पूँजी व कारोबार
	Capital and Turnover for the preceding Three Financial years with copy of latest
	Annual report.
8.	उपलब्ध वित्तीय क्षमता /ऋण सुविधाएँ
	Financial Capacity / Credit facilities available.
9.	बैंकरों के नाम व पता
	Name and Address of Bankers.
10.	व्यापार संघ जिससे उद्योग संबंधित हैं
	Trade Association to which industry belongs to
11.	संस्था/ बिक्री/जी एस टी पंजीकरण तथा पैन संख्या
	Establishment/Sales/GST Registration and PAN Number.
12.	व्यापार का प्रकार
	Nature of Business
13.	बैंकरों द्वारा जारी फर्म की सॉल्वेंसी/वित्तीय क्षमता।
	Solvency/Financial capacity of the Firm issued by their bankers
14.	उद्योग/उद्योगों की अन्य कोई जानकारी जो संगत है।
	Any other information of the industries/ies considered relevant.
15.	अपने सामर्थ्य और कमियों के क्षेत्रों को स्पष्तः उल्लेख करते हुए कंपनियों के प्रोफाइल
	The profile of the Company/ies clearly bringing out the area of Strength and
	weaknesses.
16.	ई ओ आई में भाग लेने हेतु स्वमूल्यांकन तकनीकी और संगठनात्मक क्षमता
	Self-Assessment Technical and Organisational competence to take part in the
	EOI
17.	ई ओ आई में यथा उल्लिखित प्रतिक्रिया फार्म
	Response forms as mentioned in the EOI

ई ओ आई के लिए प्रतिक्रिया में संपर्क व्यक्ति के नाम के साथ ,पदनाम, सही पता संपर्क संख्या तथा ई - मेल पते के साथ होना चाहिए।

Response to EOI must also include the name of the point of contact, together with the designation, appropriate contact number and e-mail address.

पूर्व-ई ओ आई बैठक:

पूर्व-ई ओ आई बैठक के क्रियाकलापों को अच्छी तरह समझने यदि कोई संदेह हो तो उसका निवारण करने तथा उपरोक्त क्रियाकलापों को करने हेतु अन्य तकनीकी विवरण को समझने हेतु यू आर राव उपग्रह केंद्र द्वारा एक पूर्व-बोली बैठक का आयोजन किया गया है। इच्छुक विक्रेताओं से अनुरोध है कि वे उक्त दिनांक, समय व स्थल पर पूर्व बोली बैठक में भाग लें।

Pre-Eol Meeting:

A Pre-Eol meeting is arranged by U.R. Rao Satellite Centre, Bengaluru in order to have a better understanding of the activities involved, clarify doubts if any. The interested Vendor[s] are hereby requested to take part in the Pre-Eol meeting on the Date, Time and Venue mentioned here below:

पूर्व-ई ओ आई बैठक दिनांक

Date of Pre-Eol Meeting

: 2nd जनवरी/January 2025 (गुरुवार/Thursday)

समय व स्थान/Time & Venue :	10:00 से/to 17:00 बजे/Hours IST एम ओ सी सी सम्मेलन कक्ष यू.आर .राव उपग्रह केंद्र. एच.ए.एल. एयरपोर्ट रोड, विमानपुरा डाक बेंगलूरु - 560017
	MOCC Conference Hall, U.R. Rao Satellite Centre, HAL Airport Road, Vimanapura Post, Bengaluru – 560 017.
पूर्व ई ओ आई बैठक के लिए संपर्क व्यक्ति	: क्रय व भंडार अधिकारी यू.आर .राव उपग्रह केंद्र. एच.ए.एल .एयरपोर्ट रोड, विमानपुरा डाक बेंगलूरु – 560017, कर्नाटका भारत संपर्क. 080 25084009 ई-मेल : pso_h@ursc.gov.in
Focal Point for Pre-Eol Meeting :	Purchase & Stores Officer U R Rao Satellite Centre, HAL Airport Road Bangalore – 560017, Karnataka, India Email: pso_h@ursc.gov.in Phone: 080-25084009

इच्छुक विक्रेता विनिर्दिष्ट दिनांक के पहले पूर्व बोली बैठक में भाग लेने वाले प्रतिनिधियों के विवरण सुरक्षा स्वीकृति का प्रबंध करने हेतु तालिका – 1 में विनिर्दिष्ठ संपर्क व्यक्ति को कृपया उपलब्ध करें। विक्रेता के प्रतिनिधि को पूर्व - ई ओ आई बैठक में भाग लेने हेतु "प्राधिकार पत्र" लाना होगा। बोली लगाने वाले/कंपनी/संगठन से सदस्य प्रतिनिधि, की संख्या अधिकतम केवल दो (2) तक सीमित होना चाहिए।

Vendor[s] may please provide the details of the representative[s] participating in Pre-EoI meeting well in advance prior to dates specified in Table-1 to URSC, Purchase in order to arrange for Security clearance. Vendor[s] representative shall carry an "Authorization Letter" for attending the Pre-EoI meeting. Member Representatives shall be limited to maximum of two (2) per bidder/ company/organisation.

<u>नोटः</u> आगे निविदा चरण में विक्रता(ओं) को विचार करने हेतु ई ओ आई में भाग लेना अनिवार्य है। <u>Note:</u> Participation in Eol is mandatory to consider the vendor[s] further in tendering phase.

कृपया नोट करे की किसी भी परिस्थिति में किसी भी तिथि के पूर्ववन/स्थगन नहीं किया जाएगा। Please note that request for advancement/postponement of any dates will not be entertained under any circumstances.

भाग लेने वाले इच्छुक विक्रेताओं से अनुरोध है कि वे अपने खर्च में भाग ले। यू.आर.एस.सी./इसरो द्वारा कोई परिवहन /आवास का प्रबंध नहीं किया जाएगा। The Interested Vendor[s] who are participating are required to be present on their own. No transportation/accommodation will be arranged by URSC/ISRO.

<u>टेबल/Table-1</u>

मुख्य दिनांक व समय				
Important Dat	Important Dates & Timings			
पूर्व ई ओ आई बैठक हेतु स्पष्टीकरण/पूछताछ व	31 st December 2024; 16:00 Hrs. IST			
भागीदारी विवरण की प्रस्तुति की अंतिम तिथि				
Last date of submission of clarification/				
queries & participation details for Pre				
EOI-Meeting				
पूर्व – ई ओ आई बैठक	2 nd January 2025; 10:00 to 17:00 Hrs. IST			
Pre-EOI meeting				
ई ओ आई की प्रतिक्रिया की प्रस्तुति के लिए	30 th January 2025 16:00 Hrs. IST			
अंतिम तिथि				
Last date for submission of response to Eol				
ई ओ आई के खोलने की तिथि	31 st January 2025 10:00 Hrs IST			
Opening date of Eol				

ई ओ आई के लिए संपूर्ण प्रतिक्रिया संदर्भ संख्या को स्पष्टतः उल्लेख करते हुए यू आर एस सी में नीचे दिए पते पर प्राप्त होना चाहिए तथा उपरोक्त दिनांक तथा समय के बाद नहीं।

Complete response to EOI, clearly super scribing the reference Number and due date of EOI, must be received at URSC to the address given below, not later than the date and time specified above.

a. प्रधान, क्रय व भंडार Sr. Head, Purchase & Stores यू आर राव उपग्रह केन्द्र U R Rao Satellite Centre, एच ए एल एयरपोर्ट रोड HAL Airport Road, बेंगलूरु -560017, भारत Bangalore – 560017, India

बिना कारण बताएं "इच्छा की अभिव्यक्ति" को स्वीकार या अस्वीकार करने का अधिकार यू आर एस सी आरक्षित रखता है।

URSC reserves the right to accept or reject all or any such "Expression of Interest" without assigning any reasons what so ever.

Disclaimer: The English version shall always prevail in case any discrepancy or inconsistency between English and Hindi version of this Invitation.

Sd/-वरिष्ठ प्रधान, क्रय व भंडार/ Sr. Head, Purchase & Stores

EXPRESSION OF INTEREST (Eol)

FOR REALISATION OF INTEGRATED MODULAR POWER PACKAGES (IMPP) FOR 100V BUS

November 2024

Prepared by

POWER SYSTEMS GROUP URSC/ISRO

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i. ABBREVIATIONS USED:

AI	Aluminium
ATE	Automated Test Equipment
ASIC	Application Specific Integrated Circuit
BCR	Battery Charge Regulator
BCS	Battery Current Sensor
BDR	Battery Discharge Regulator
BLL	Bus Live Lug
BOM	Bill of Material
BRL	Bus Return Lug
BSR	Boost Shunt Regulator
CC	Capacitor card
COC	Certificate Of Compliance
CPE	Core Power Electronics
CVCM	Collected Volatile Condensable matter
DC	Direct Current
DDR	Detailed Design Review
DomReg	Domestic Regulator
DR	Discharge Relay
EEE	Electrical and Electronic & Electromechanical
EIDP	End item data pack
EOC	End of Charge
EOI	Expression of Interest
EMI	Electromagnetic Interference
EMC	Electromagnetic Compatibility
ECAD	Electronics Computer Aided Design
EM	Engineering Model
EMI	Electro Magnetic Interference
EMC	Electro Magnetic Compatibility
ESD	Electro Static Discharge
ESR	Effective Series Resistance
FM	Flight Model
FPGA	Field Programmable Gate Array
FRB	Flat Ribbon Board
HMC	Hybrid Micro Circuit
H/W	Hardware
IBT	Integrated Bench Tests
ICM	Individual Cell Monitoring
I-6k	ISRO-6 ton kilogram class
IC	Integrated Circuit
IMPP	Integrated modular Power Packages
ISRO	Indian Space Research Organization
I/P	Input

kW	kilo watt
LCS	Load Current Sensor
LTP	Lower Trip Point
MB	Mother Board
MIL-STD	Military Standard
MOQ	Minimum Order Quantity
MVL	Majority Voting Logic
NDA	Non-Disclosure Agreement
OEM	Original Equipment Manufacturer
O/P	Output
OVP	Over Voltage Protection
PCB	Printed Circuit Board
PCU	Power Conditioning Unit
PDR	Preliminary Design Review
PID	Process Identification Document
PI	Power Integrity
Pkg	Package
PM	Power Module
PO	Purchase Order
PWM	Pulse Width Modulation
QM	Qualification Model
Redt	Redundant
SAR	Solar Array Regulator
SI	Signal Integrity
SIM	Simulator
SMD	Surface Mount Device
T&E	Test & Evaluation
SMT	Surface Mount Technology
ТМ	Telemetry
тс	Telecommand
TIM	Thermal interface material
URSC	UR Rao Satellite Centre
UTP	Upper Trip Point
UUT	Unit under Test

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PART- 1 1.0 GENERAL INFORMATION

2.0 OBJECTIVE:

ISRO is embarking on a mission to produce large number of satellites to be put in orbit in the next five years and is all set to realize 15 to 20spacecraft per year. This calls for a large number of electronic sub-systems to be fabricated, tested and made ready for integration. In order to meet the growing demand of high power satellites, it becomes imperative to realise a high power& high voltage power bus capable of handling output power of 10- 20 kW. A high voltage (100V), high power, modular and optimized power package for I-6k satellite platforms has been envisaged and proposed in this document.

U.R. Rao Satellite Centre (URSC) is currently developing Integrated Modular Power Packages (IMPP) for 100V Bus. For the realisation of IMPP, URSC is looking for the support of Indian industry with strong engineering, design and analysis background for the delivery of 3 sets of Engineering Model (EM) hardware.

3.0 SCOPE OF WORK:

URSC invites application for Expression of Interest (EoI) with a detailed proposal along with proof of vendor expertise to develop EM of IMPP for 100V power bus. After successful demonstration of first EM, subsequent EMs(2Nos) shall be realised, tested and delivered by incorporating the suggestions/observations made during first EM model evaluation. This document provides the basic information needed for expression of Interest related to IMPP for 100V bus. It further specifies vendor selection criteria, EoI proposal, indent process, design details, list of activities to be carried out and the responsibility of vendor and URSC in executing this work.

The activities to be carried out by the vendor for the realisation of IMPP are the following

- Mechanical housing design and analysis using aluminum alloy (AA6061) for 20kW of output power and realization for 10kW.
- PCB layout design for the circuit schematic provided
- Verification of PCB design using appropriate software tools.
- EEE component procurement and storage
- Special test equipment procurement
- PCB fabrication
- SMT and through hole fabrication
- Testing of cards and packages as per the specifications
- Tuning of design to meet the specifications
- Assembly of all the individual modules to form IMPP
- Environmental testing at module and integrated levelas per the test levels provided

• Final Integrated bench testing of IMPP as per the specification

This hardware is planned to be realized through qualified vendors who are familiar and have experience in aero space electronic hardware realization and who own necessary infrastructure for fabrication, testing, simulation/analysis and experience of handling high reliability (HIREL) EEE components.

4.0 INTRODUCTION TO INTEGRATED MODULAR POWER PACKAGES FOR 100V BUS:

This section gives a brief introduction regarding the functional aspects of different types of power electronics packages used in 100V IMPP. Figure 1.1 gives the block diagram of the proposed unit.

IMPP for 100V power bus contains a single power stack PCU and battery electronics modules. PCU contains the following cards/packages/modules.

- 1. Domestic regulator
- 2. Bus-bar
- 3. Bus Capacitor
- 4. Majority Voting Logic (MVL)
- 5. Decoder
- 6. FPGA
- 7. Boost Shunt Regulator (BSR)
- 8. Battery Charge Regulator (BCR)
- 9. Power Module (Battery Discharge Regulator +Shuntswitch)
- 10. Load current sensor (LCS)
- 11. Domestic Regulator OVP& TM (DROVP)
- 12. Mother boards

The Battery Electronics module contains the following packages.

- 1. Individual cell monitoring (ICM)
- 2. Battery current sensor (BCS)
- 3. Self-bias DC-DC converters

The 100V PCU shall be designed to be of modular in construction with the modules interconnected by a mother board. The bus live and return shall be formed using insulated bus-bar.



Fig 1.1: Block diagram of IMPP for 100V bus

5.0 VENDOR SELECTION CRITERIA

The vendor selection is a process to ensure that only industries with the capability to realise Power electronics modules in the range of 10kW of output Power along with necessary mechanical housing design, PCB design, necessary analysis capability shall be part of this activities.

A detailed list of the vendor qualification criterion is provided in the table 1.4. The interested industries shall produce necessary documentary evidence to prove their capability to execute the above H/W(hardware) at the time of EoI submission. These responses will be evaluated by URSC and those vendors who are eligible based on the data provided will be selected. It may be noted that, Industries cannot participate directly in the RFP, if they have not participated in the EoI.

Vendors shall fulfil the following requirements to become eligible to participate in the EoI, for end to end realization of 3 EM models of 100V Bus IMPP, as per the definition of work.

SI	Criterion	Proof	Remarks
1	Experience in design and analysis of mechanical housing for high power (at least 1kW per module)	Purchase order with a certification for successful completion OR Vendor should have a product present in the company catalogue /website meeting the requirement. OR Shall provide information on a product under development which can be demonstrated within a short time. OR The vendor shall produce a letter of intent or valid MoU with other entity/organisation.	The activity shall involve mechanical package design and Vendor shall demonstrate the product based on URSC request
2	Experience in PCB layout and multilayer PCB design of high power (at least 1kW), high density, mixed signal PCBs	Purchase order with a certification for successful completion OR	The activity shall involve PCB design and Vendor shall

SI	Criterion	Proof	Remarks
No			
		Vendor should have a product present in the company catalogue /website meeting the requirement. OR Shall provide information on a product under development which can be demonstrated within a short time OR The vendor shall produce a letter of intent or valid MoU withother entity/organisation.	demonstrate the product based on URSC request
3.	Experience in fine tuning and evaluation of design and expertise in closed loop stability analysis of electronic circuit using ATE or other equipments.	Shall produce documentary evidence on any product already designed or under development which can be demonstrated on demand.	
4	Should have experience in realization or procurement of PCBs, Mechanical Housings and Consumables for realization of avionics hardware.	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement.	
5	Organization should be capable of procuring the EEE Parts from OEM/Authorized Distributors as identified for realization of the above hardware. Vendors should have experience in storage and handling of EEE parts.	Purchase order with a certification for successful completion.	
6	Organization Should have	Analysis reports carried	

SI	Criterion	Proof	Remarks
	experience in the following analysis Signal integrity (SI) analysis Power integrity (PI) analysis EMI-EMC analysis PCB and package level thermal analysis in conduction and radiation	out by the organisation internally on any package on modules having power of around 1KW for SI, PI analysis (frequency 24 MHz), power dissipation greater than 100W in one module for thermal analysis with only conduction and radiative cooling.	
	 Mechanical analysis for vibration/Modal analysis Reliability assessment FMECA & FTA Worst Case circuit Analysis De-rating analysis Reliability prediction number 	OR The vendor shall produce a letter of intent or valid MoU with other entity/organisation.	
7	Organization shall provide details about their experience for the design, analysis and fabrication of Insulated bus-bar to meet the specifications provided by URSC.	This requirements can be met by the vendor or shall produce a letter of intent to collaborate or a valid MoU with other entity	
8	Organisation should have Experience in MIL-STD-1553 based designs	Purchase order with a certification for successful completion. OR Vendor should have a product present in the company catalogue /website meeting the requirement. OR Shall provide information on a product under development which can be	

SI No	Criterion	Proof	Remarks
		demonstrated within a short notice.	
9	SMT (Surface Mount Technology)facility	Documentary Proof of certified facility or letter of intent or valid MoU with other entity/organisation	Organization can use their own / other vendor facilities or use ISRO facility through INSPACE.
10	Environmental test Facility(Hot and cold ,Thermal vacuum)	Documentary Proof of certified facility or letter of intent or a valid MoU with other entity/organisation	Organization can use their own / other vendor facilities or use ISRO facility through INSPACE.
11	Experience in generating design requirements /design and development of automated test equipment for Electronics packages having capability to interface through standard protocols for instrument control and through 1553 B with UUT.	Purchase order with a certification for successful completion /design document for similar in- house development. OR Shall produce a letter of intent to collaborate/support with the vendor	
12	Experience in package level testing of electronics packages.	Purchase order with a certification for successful completion	
13	Should have an ESD safe laboratory and of minimum space >100 square meter, certified by URSC/SAC or NABL accredited with ISO/ AS9100 certification which can be inspected.	Proof of certification shall be produced.	URSC may inspect the facility to verify compliance.
14	Organisation should have	Purchase order with a	Vendor shall

SI	Criterion	Proof	Remarks
No			
	experience in conducting EMI- EMC tests and qualifying products as per MIL-STD 461C/E/F/G	certification for successful completion. OR letter of intent or valid MoU with other entity/organisation	provide analysis reports.
15	Organisation should have experience in designing for vibration specification as per MIL-STD-810/DO-160G and conducting vibration tests	Purchase order with a certification for successful completion. OR Shall produce a letter of intent or valid MoU with other entity/organisation	Vendor shall provide analysis reports.
16	Vendor should have a static IP address.	Necessary proof shall be provided	
17	Organisation shall sign a Non- Disclosure agreement with URSC immediately after PO release.	To be complied	

Table 1.1 Vendor selection criteria

6.0 EOI PROPOSAL

Vendor selection is strictly based on the documentary proof and compliance requirement as mentioned at table No. 1.1 Vendor shall also submit response for Eol proposal/plans along with documentary evidence, wherever applicable. The following table gives the details about the proposal.

SI	Document name	Remarks
No.		
1	Organisation structure	To be provided
2	Vendor's Project structure	This shall include roles and responsibilities for
		executing this requirement
3	Vendor capability and	Documentary evidence and Compliance for
	Compliance	vendor selection/qualification criterion as per
		table 1.1 and nature of work as per section 9.0
		of this document
4	Project plan	Shall contain the following

SI	Document name	Remarks
NO.		 Work break down structure (Concept to delivery) Schedule for EM1, EM2 and EM3 realisation Gantt chart & critical path suggestions to reduce the critical issues
5	List of organisations/Collaborations	Details of organisations/companies who will be collaborating with the vendor in the form of letter of Intent or valid MoU. Vendor should be responsible for final project and product outcome.
6	Detailed list of analysis	 Following questions need to be addressed for each analysis Stage at which the analysis shall be performed. Software/tools which will be used for the analysis Which entity will be performing the analysis.
7	PCB design	EMI-EMC plan and stage of analysis.
8	PCB fabrication &assembly plan	The document shall contain all details & process from PCB fabrication to conformal coating, potting and radiation shielding along with TIM(Thermal interface material) implementation
9	Mechanical hardware fabrication and assembly plan.	The document shall contain design, material fabrication, process activities (thermal and mechanical), procurement and assembly with PCB along with thermal implementation.
10	Procurement plan for EEE parts	Procurement plan shall be given/presented
11	List of software proposed	This document shall provide all the software required to carry out the listed analysis/ activity. Software availability with organisation or letter of Intent/ MoU details with other entities or procurement plan shall be mentioned. Refer Annexure A for analysis format at list of deliverables.

Table 1.2 Eol proposal

7.0 Eol/INDENTING PROCESS:

Expression of Interest (EoI) for identifying a suitable vendor for the realisation of 3 EM Models will have a pre-bid meeting where vendors will be briefed regarding the indenting process. Preliminary design details, block diagram, Bill of Materials(BoM) and details required to make a proposal is provided in this document. Participation in pre bid meeting is not mandatory for participation in EoI proposal submission.

A detailed vendor selection criterion is provided at table 1.4.for which interested vendors are required to provide all the documentary proofs as per the list.

Based on the data, vendor is expected to give a detailed proposal with all technical details along with project execution plan. A presentation from vendor may be sought to understand the proposal, if necessary. All responses will be evaluated by URSC and a list of qualified vendors will be made.

An indenting process will be initiated in a Limited tender mode only among the qualified vendors whose EoI is found satisfactory for the above work. A flow chart of the EoI process mentioned in Fig 1.4



Fig. 1.2: Eol process flow chart

8.0 REALISATION METHODOLOGY

The goal of this development is to deliver a single power stack (Power control unit) consisting of all power electronics hardware and battery related PE packages. It is planned, to realise this hardware with a weight of around 40kgs for 10kW of output power with an approximate dimension of 570x380x320 mm³. The design should be scalable to meet output power of 20kW with an approximate weight of around 60kg

with a dimension of 800x380x320mm³. All electronic circuits in the power control unit is divided into two categories.

B C R	B S R	B S R	P M	P M	P M	Р М	CPE	Р М	P M	P M	P M	B S R	B C R	B C R	
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						-	

- ✓ Power conditioners
- \checkmark Core power electronics

PM= Power module; BCR = Battery charge regulator;

BSR = Boost shunt regulator; CPE = Core power electronics

8.1 Power Conditioning unit (PCU)

Power module, BSR and BCR are the power conditioners. Power Module consist of 1 BDR with either 1 or 2 ON/OFF strings depending on string capacity such that single module will be providing power irrespective of sun light or eclipse. Power Module will handle 1.25KW during eclipse and 2kW (approx.) will be handled during sun light.

8.2 Core Power Electronics (CPE)

Core Power electronics consists of Domestic Regulator, Bus capacitor, MVL, Decoder, FPGA, LCS and DROVP. Signal Interface between CPE cards/modules/packages will be through suitable interface. Signal interface between power conditioners and CPE will be through suitable interfaces.For external communication, 1553B protocol shall be used.

Modules	No. of modules required for
	10kW Output Power
PM(BDR+ Shunt)	8
BCR	3
BSR	3
Core power	1

Table 1.3: No of modules required for PCU – 10kW of output Power

Indicative stacking diagram of battery PE packages is mentioned at Fig 1.4

Modules	No. of modules required for
	10kW Output Power
BCS	2
ICM	3
Self Bias DCDC	1

Table 1.4 No of modules required for Battery PE Pkges



Fig 1.4 Indicative stacking diagram for Battery PE packages

No. of modules required for Battery electronics module is mentioned at Table No. 1.4

Note:1. For battery related PE hardware, circuit schematics, Mechanical design drawings and.dxf files will be provided by URSC.

2. Mechanical design analysis is not needed for Battery modules

The details of total packages needed for 100V IMPP for Output Power of 10kW and 20kW are consolidated and mentioned at table 1.5

SI. No.	Name of card/Pkg/Module	Qty for 10kW	Qty for 20kW	Remarks
01	Power Module	8	16	
02	Bus Capacitor	2	2	
03	Majority Voting Logic (MVL)	1	1	
04	Boost shunt regulator(BSR)	3	3	
05	Decoder	1	1	
06	FPGA	2	2	Main +Redt
07	Domestic regulator	2 *	2*	Main +Redt
08	Load current sensor(LCS)	2	2	
09	Battery charge regulator(BCR)	3	3	
10	ICM	3	3	Part of battery
11	BCS	2	2	Part of battery
12	Self-bias DC/DC	2*	2*	Part of battery
13	Mother Board	\$	\$	
14	Bus bar	#	#	
15	DROVP	1	1	

Table 1.5: No. of Modules required for 10kW and 20kW IMPP for 100V bus

Note: No of packages needed for 20kW of output power in the above table is for understanding the scalability requirement and to provide various Electrical and mechanical analysis mentioned at Table 1.1 and annexure A

* Built to specifications
For interconnection of the packages
\$ - May vary based on the module/package design.

9.0 NATURE OF WORK

Realisation of 100V IMPP is divided into three phases.

1.Configuration phase

- Initial phase starts after the PO is placed and NDA (Non-Disclosure Agreement) is signed between vendor and URSC.
- Schematics, Bill of material and Major specifications of the board & package for all the boards will be provided by URSC. Any suggestions or improvements can be proposed by vendor. Final decision to accept the proposal in part, total or to reject it is at URSC discretion.
- Vendor needs to carry out initial assessment of package, card level dimensions, PCB design, Mechanical housing design, assessment and implementation of thermal management scheme etc. to ensure that the mass and dimensions are met. After design finalization by the vendor, a joint Baseline Design Review (BDR) will be held by vendor to obtain clearance from URSC.

Following aspects shall be discussed at the BDR stage:

- Configuration of the IMPP
- Rationale for arriving at a particular PCB and mechanical design/modifications
- Schematic tuning/change (reason and rationale for the change)
- PCB/mechanical housing design guidelines
- Thermal management plan
- EMI-EMC plan
- Test system (Automated Test Equipment) plan
- Test philosophy
- Project execution plan and schedule
- Process Identification Document (PID)
- Procurement plan

2. Design and Analysis phase

After clearance from URSC, the vendor shall initiate card/board layout followed by below mentioned analysis for electronics/mechanical designs. (Refer Annexure- A)

- Signal integrity analysis
- Power integrity analysis
- PI & Thermal co-simulation
- Card/package level thermal analysis
- Card/package level structural analysis
- Reliability assessment
 - FMECA & FTA
 - Worst Case circuit Analysis
 - De-rating analysis
 - o Reliability prediction number
- EMI/EMC analysis etc

Vendor shall initiate mechanical design and carry out package level structural & thermal analysis and ensure designs shall meet the required specifications. After all the design objectives are met, vendor shall hold a joint **Detailed Design Review (DDR)** with URSC to obtain the clearance to proceed further. DDR shall include review of the following activities.

- PCB design placement and routing
- Review of schematic changes, if any
- Signal integrity (SI) analysis
- Power integrity (PI) analysis
- EMI-EMC analysis
- PCB and package level thermal analysis in conduction and radiation modes
- PCB and package level Mechanical analysis for vibration/Modal analysis
- Reliability assessment
 - FMECA & FTA
 - Worst Case circuit Analysis
 - o De-rating analysis
 - Reliability prediction number
- Test system adequacy
- Test case list
- Component procurement process
- Fabrication process
- Project plan and schedule
- PID

Note: DDR clearance is a mandatory requirement to continue for further activities

3. Realization and testing phase

- Vendor shall carry out component procurement, PCB fabrication, mechanical housing fabrication, wiring of the cards, card level and package level testing at vendor's premises for initial clearance using vendor's test equipment. Test Equipment used by vendor for initial clearance shall be vendor's responsibility. Vendor shall hold a joint first model(EM-1) test results review with URSC and obtain the clearance to proceed further.
- Materials and process shall be TML and CVCM compliant.
- Failure of components during any phase of the project shall be reported to URSC and required analysis shall be carried out.
- Test results review shall include a review of the following activities
 - Fabrication reports review
 - Process review
 - Test results review
 - PID
- Functional verification testing will be carried out by URSC to ensure all the design parameters are met or as expected and to bring out any design issues.
- Any issues observed during the first model (EM-1) testing need to be addressed, resolved and reviewed before proceeding to fabrication and delivery of second model and third model (EM2 &3) with necessary corrective implementation as observed during first model(EM-1) testing. Incremental analysis required shall be carried out by the vendor.

10.0 ROLE & RESPONSIBILITY OF VENDOR & URSC

SL.	SUBJECT/DESCRIPTION	Responsibility
No.		
1.	Schedule Planning	Vendor
2.	Components Procurement	Vendor
3.	Electrical design clearance during BDR, DDR and Clearance of Procured Components for use	URSC
4.	EEE Components Storage and Handling	Vendor
5.	Procurement of fabrication tools and equipment	Vendor
6.	Mech.Housing design	Vendor
7.	Procurement of PCBs, Mechanical assemblies and consumables.	Vendor
8.	Audit/ Clearance of PCB Layout, PCB's, mechanical design analysis and Mechanical Housings	URSC
9.	Test Equipment, Test Jigs Procurement & Calibration	Vendor

Role and responsibility of vendor and URSC in mentioned in table 1.6

10.	Package level Test System design evaluation and clearance	URSC
11.	Facility audit & clearance	URSC
12.	Production document preparation	Vendor
13.	Production Document Approval	URSC
14.	Review Board for material /process/fabrication	Vendor
15.	Review Board for design/testing/non conformance	Vendor
16.	Approval of disposition from vendor review boards	URSC
17.	Focal point for work status reporting	Vendor
18.	Testing and documentation	Vendor
19.	Independent T&E (Test & Evaluation)	Vendor
20.	Approval of Test Results	URSC
21.	End Item Data Package (EIDP) including scanned copies of all fabrication/test folders	Vendor
22.	Log Books, Folders & File Maintenance and Submission of same to URSC along with hardware.	Vendor

Table 1.6 Responsibilities - URSC& Vendor

11.0 LIST OF DELIVERABLES BY VENDOR

The list of deliverables from vendor at each phases are as follows:

S. No.	Deliverables			
I.	Electrical, thermal and mechanical analysis report			
	 For EEE components: a. Part details such as part number, package style etc being procured b. Other requirements such as CoC(Certificate of compliance) and authorization letter. 			
11.	Mech. Housing and PCB design details or procurement details. The design should be available in the following formats. Schematic- ORCAD *.dsn PCB – Cadence with *.brd Mechanical design - *.prt Thermal design - *.idx Test console software – Lab view based source code PCB design and fabrication to be carried as per ISRO-PAX-301. Acceptance certificate of Mech. housing and PCB			

	Equipment Calibration and validity certificates		
III.	Fabrication / assembly folders for cards/ packages and		
	inspection reports (both hard and soft form)		
IV.	Card Level Test Results		
V.	Initial bench test results.		
VI.	Environmental test results.		
VII.	Final bench test results.		
	Fabricated and tested packages/electronic hardware with		
	certificates		
	Package Level Test Systems details.		
VIII.	Re-test Results if applicable & delivery of hardware along with		
	revised Certificate and EIDP		

Table 1.7: List of deliverables by vendor

12.0 APPLICABLE DOCUMENTS/ STANDARDS

The documents mentioned at Annexure-C shall serve as reference documents/standards for this contract. This documents cover various phases of activity including workmanship standards, schematic design guidelines, non conformance control, failure reporting, ESD control, production assurance guidelines, EEE components management, de-rating guidelines, EMI/EMC test standards, thermal design and analysis, reliability prediction and guidelines for environmental tests. Vendors shall comply with all the requirements mentioned in these documents.

PART-2

13. TECHNICAL INFORMATION

(CARD/MODULE /PACKAGE SPECIFIC)

13.1 Name of Design: Power Module (PM)

a. Brief Description/functionality of module:

The Power Module (PM) is responsible for processing power from battery as well as solar array. The PM is modular in nature to meet the different load power requirements of various spacecraft configuration. Each PM can process around 1.25 kW of battery power and 2 kW of solar array power with 100V as the output. The battery power processing is done through a DC-DC converter whereas the solar array power is processed using a shunt regulator.

b. Block diagram:



Fig. 1.5 Block diagram – Power Module

c. Powering scheme:

PM receives bias supplies such as +14.7V, -14.7V, 5.7V & +12.7V from the domestic regulator for powering all the ICs present in PM and driving of MOSFETs. Two chain of bias supplies are required for redundancy purpose. Two hot redundant domestic regulators are used for providing two chains of bias supplies through back plane interfaces. No sequencing is required among the bias supplies and all are expected to be available at PM at the same time.

d. Grounding scheme:

Power module processes the battery power as well as solar array power. The power ground is isolated in the module from the bias supply ground. Since Distributed

Single Point Grounding Scheme (DSPG) is followed, the bias grounds will get connected to the chassis of the module. +12.7V bias supply return will be connected to bus negative due to +12.7V utilisation in the circuit.

e. Power handling and dissipation:

Power Module handles 1250W of battery power and 2000W of solar array power. The module should able to handle maximum power dissipation of 45W.

f. No of modules:

For the planned 3 EM models of PCU for handling 10KW of output power, 8 power modules are required (with one module as redundant) to process the battery power. These modules are modular in nature and share the total power among themselves.

g. Interface Details:

i. Input Signals:

SI No	Description	Remarks
1.	Battery Live & Return Input	66V – 96V
2.	Solar Array Live & Return Input	0V – 105V
3.	Bias Supply	±14.7V,5.5V,12.7V
4.	MVL Signal	±11V
5.	Tele-command	28V & 5V 64ms pulse, 5V level

Table 1.8: Input signals – PM Module

ii. Output Signals:

SI No	Description	remarks
1.	Bus Live & Return Output	99V-103V
2.	Telemetries	0V-5V

Table 1.9: Output signals – PM Module

h. Component List:

PART NO	QTY
CDR31 1 KPF +/-10% TC +15%-25% 100V	2
CDR31 10 KPF +/-10% TC +15%-25% 50V	1
CDR31 2.2 KPF +/-10% TC +15%-25% 100V	1
CDR31 8.2 KPF +/-10% TC +15%-25% 50V	5
CDR32 1 KPF +/-1% 30 PPM 100V	2
CDR32 12 KPF +/-10% TC +15%-25% 100V	1
CDR32 2.2 KPF +/-5% 30 PPM 50V	4
CDR32 27 KPF +/-10% TC +15%-25% 50V	1

CDR32 8.2 KPF +/-10% TC +15%-25% 100V	2
CDR33 0.1 UF +/-10% TC +15%-25% 50V	21
CDR33 47 KPF +/-10% TC +15%-25% 50V	1
CDR35 0.22 UF +/-10% TC +15%-25% 50V	4
CDR35 0.47 UF +/-10% TC +15%-25% 50V	5
CWR06 1 UF 5% 35V SNPB	1
CWR29 22 UF 5% 25V SNPB-CASEH	3
MLCC1206 47 KPF 10% 200V	4
DSUB-COMBO-POWER-5W5M-90	1
FRB-44-MC	1
55548-W4	1
YP-41306-TC	5
YW-40907-TC	3
1N4569-SMD	1
1N4625-SMD	2
1N4626-SMD	4
1N4964-SMD	3
1N5806-SMD	21
1N5811-SMD	2
1N6642-SMD	41
1N945-SMD	2
FM12A-15A-135V-RADIAL	7
111-CFP10	2
124-SOP14	2
139-CFP14	1
1825-CFP16	1
1845A-DIP8	2
4013B-CFP14	1
4424-MBCFP16	3
GP250-720-EDB-26V-L-CAN2	1
RM0505 1 KOHM 1% 100 PPM 1/8W	3
RM0505 1.21 KOHM 1% 100 PPM 1/8W	4
RM0505 10 KOHM 1% 100 PPM 1/8W	15
RM0505 100 KOHM 1% 100 PPM 1/8W	5
RM0505 12.1 KOHM 1% 100 PPM 1/8W	2
RM0505 15 KOHM 1% 100 PPM 1/8W	1
RM0505 150 KOHM 1% 100 PPM 1/8W	3
RM0505 4.12 KOHM 1% 100 PPM 1/8W	1
RM0505 4.75 KOHM 1% 100 PPM 1/8W	18
RM0505 47.5 KOHM 1% 100 PPM 1/8W	1
RM0505 5.11 KOHM 1% 100 PPM 1/8W	1
RM0505 5.76 KOHM 1% 100 PPM 1/8W	1
RM0505 57.6 KOHM 1% 100 PPM 1/8W	1
RM0505 8.25 KOHM 1% 100 PPM 1/8W	1

	9
RM1206 1.5 KOHM 1% 100 PPM 1/4W	1
RM1206 10 KOHM 1% 100 PPM 1/4W	5
RM1206 10 OHM 1% 100 PPM 1/4W	4
RM1206 100 KOHM 1% 100 PPM 1/4W	1
RM1206 110 KOHM 1% 100 PPM 1/4W	4
RM1206 12.1 KOHM 1% 100 PPM 1/4W	1
RM1206 121 KOHM 1% 100 PPM 1/4W	4
RM1206 14.7 KOHM 1% 100 PPM 1/4W	1
RM1206 18.2 OHM 1% 100 PPM 1/4W	3
RM1206 182 KOHM 1% 100 PPM 1/4W	1
RM1206 2 KOHM 1% 100 PPM 1/4W	2
RM1206 2.21 KOHM 1% 100 PPM 1/4W	1
RM1206 2.67 KOHM 1% 100 PPM 1/4W	1
RM1206 20 KOHM 1% 100 PPM 1/4W	5
RM1206 200 OHM 1% 100 PPM 1/4W	1
RM1206 22.1 KOHM 1% 100 PPM 1/4W	4
RM1206 221 OHM 1% 100 PPM 1/4W	1
RM1206 24.3 KOHM 1% 100 PPM 1/4W	1
RM1206 27.4 KOHM 1% 100 PPM 1/4W	1
RM1206 3.01 KOHM 1% 100 PPM 1/4W	1
RM1206 33.2 KOHM 1% 100 PPM 1/4W	1
RM1206 332 OHM 1% 100 PPM 1/4W	2
RM1206 4.75 KOHM 1% 100 PPM 1/4W	3
RM1206 4.99 KOHM 1% 100 PPM 1/4W	3
RM1206 47.5 KOHM 1% 100 PPM 1/4W	4
RM1206 5.11 KOHM 1% 100 PPM 1/4W	1
RM1206 5.62 KOHM 1% 100 PPM 1/4W	1
RM1206 6.19 KOHM 1% 100 PPM 1/4W	1
RM1206 6.49 KOHM 1% 100 PPM 1/4W	2
RM1206 6.81 KOHM 1% 100 PPM 1/4W	4
RM1206 75 KOHM 1% 100 PPM 1/4W	4
RM1206 8.25 KOHM 1% 100 PPM 1/4W	3
RWR80N 10 OHM 1% 2W	4
RWR80N 182 OHM 1% 2W	3
RWR80N 221 OHM 1% 2W	8
RWR80N 3.01 KOHM 1% 2W	2
RWR80N 3.01 OHM 1% 2W	5
2N3637-SMD	1
2N3700-SMD	1
2N5666-TO5	1
DSUB-COMBO-5W5M	1
58324-A2	1
ZP-43615-TC	1

35CGQ150-TO254	10
EL215-147-A-28V-L-CAN3	1

Table 1.10: component List – PM Module

13.2. Name of Design: Bus Capacitor

a. Brief Description/functionality of module:

The power bus provided to the user should have low impedance at the source. This low impedance of the bus is achieved by having sufficient low ESR capacitors. Capacitor bank is designed to do exactly the same job. The complete capacitor bank consist of 2 capacitor cards. Spacecraft is made ON using bus simulator concept. The interface of bus simulator to spacecraft power bus is housed along with the capacitor bank. The Power Conditioning Unit (PCU) requires bus voltage as feedback and powering the Domestic regulators. Fused bus voltage signal for these requirements are provided with this card.

b. Block diagram:



Fig. 1.6 Block diagram - Bus Capacitor card

c. Powering scheme:

The capacitor card doesn't contain any circuit which requires any biasing. Powering this card is via bus simulator input or directly connecting across the bus.

d. Grounding scheme:

Since this PCB doesn't contain any circuit which requires any biasing, it doesn't require any signal grounding scheme. The bus return present in the card is connected to bus bar return and doesn't require any grounding with respect to chassis.

e. Power handling and dissipation:

Since this PCB hold the capacitor bank for the bus, it doesn't require any specification related to power handling. All the power handled by this module are transient in nature. The PCB should be designed to handle power dissipation of the order of 2W. The bus simulator interface which interface the PCU with ground equipment shall dissipate a power of 8W. This power dissipation is only during ground operation and not during mission or inflight.

f. No of modules:

Two such modules are required for meeting the bus capacitance requirements.

g. Interface Details:

i. Input Signals:

SI No	Description	remarks
1.	Bus Simulator Live & Return Input	0V – 105V

Table 1.11: Input signal - Capacitor card

ii. Bi-directional Signals:

SI No	Description	remarks
1.	Bus Live & Return Input	0V – 105V

Table 1.12: Bidirectional signal - Capacitor card

iii.Output Signals:

SI No	Description	remarks
1.	Fused Bus Live & Return outputs	0V – 105V

Table 1.13: Output signal - Capacitor card

h. Component List

PART NO	QTY.
DSUB-COMBO-POWER-3W3F-90	2
DSUB-COMBO-POWER-3W3M-90	1
DSUBN-15S-PCB-90L5	1
FM12A-10A-135V-RADIAL	1
FM12A-5A-135V-RADIAL	2

RM1206 150 KOHM 1% 100 PPM 1/4W	8
5CGQ150-TO254	2
RM1206 150 KOHM 1% 100 PPM 1/4W	8
PM907NS 100UF 10% 170V-PM907S	26
FM13-0.5A-125V-SMD	5
DSUB-COMBO-POWER-3W3F-90	2
DSUB-COMBO-POWER-3W3M-90	1
DSUBN-15S-PCB-90L5	1
FM12A-10A-135V-RADIAL	1
FM12A-5A-135V-RADIAL	2
RM1206 150 KOHM 1% 100 PPM 1/4W	8
5CGQ150-TO254	2
RM1206 150 KOHM 1% 100 PPM 1/4W	8
PM907NS 100UF 10% 170V-PM907S	26
FM13-0.5A-125V-SMD	5

Table 1.14: Component List - Bus Capacitor card

13.3. Name of Design: Majority Voting Logic Card (MVL)

a. Brief Description/functionality of module:

The Battery Discharge Regulator (BDR) & Solar Array Regulator (SAR) regulates the bus voltage to a set point through a closed loop system. The voltage feedback for both BDR & SAR becomes very crucial for to achieve fully regulated power bus. For this reason the voltage feedback system is generated by a majority voting logic (MVL) circuit. Along with the two MVL circuits, one each for BDR & SAR, MVL card contains power bus voltage telemetry circuits and bus over voltage detection and control signal generation circuit for external loads.

b. Block diagram:

The block diagram of MVL card is shown in Fig. 1.7

c. Powering scheme: MVL receives bias supplies such as +14.7V & -14.7V from the domestic regulator for powering all the ICs. Two chain of bias supplies are required for redundancy purpose. Two hot redundant domestic regulators are used for providing two chain of bias supplies through back plane interfaces. No sequencing is required among the bias supplies and all are expected to available at MVL card at the same time.



Fig. 1.7 Block diagram – Majority Voting Logic (MVL)

d. Grounding scheme:

MVL card receives fused bus voltage for sensing purpose. These signals are referred to the signal ground rather than the power ground. Two grounding plane is required in this board to have isolation between BDR MVL and SAR MVL. BDR MVL circuit is connected to a ground plane which has provision to get either referred to signal ground in the PCB or to power ground through the interfacing connector. All the remaining circuits in the PCB are referred to the signal ground and can have connection with chassis of the package. This grounding follows the DSPG scheme.

e. Power handling and dissipation:

The electronics present in this board are for analog signal processing. The PCB should be designed to take care of heat dissipation of 3W.

f. No of modules: Single MVL is planned for PCU.

g. Interface Details:

i. Inp	ut Signals:
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SI No	Description	remarks
1.	Bus Live & Return Input	0V – 110V
2.	Battery Sense live	66V - 96.6V
3.	Bias Supply	±14.7V

Table 1.15: Input signal – MVL card

ii. Output Signals:

SI No	Description	remarks
1.	MVL Signals	±11V
2.	Telemetries	0V-5V
3.	Battery Sense live	66V - 96.6V
4.	BUS OVP signal	±14V

Table 1.16: Output signal – MVL card

h. Component List:

CDR33 0.1 UF +/-10% TC +15%-25% 50V	50
CKR05 180 PF 10% 200V	2
DSUBN-25P-PCB-90L5	2
FRB-44-MC	2
1N4569-SMD	12
1N4626-SMD	4
1N6642-SMD	26
1N945-SMD	12
111-CFP10	12
124-SOP14	8
RM1206 1 KOHM 1% 100 PPM 1/4W	12
RM1206 10 KOHM 1% 100 PPM 1/4W	34
RM1206 100 KOHM 1% 100 PPM 1/4W	8
RM1206 12.1 KOHM 1% 100 PPM 1/4W	6
RM1206 140 KOHM 1% 100 PPM 1/4W	4
RM1206 147 KOHM 1% 100 PPM 1/4W	6
RM1206 15 KOHM 1% 100 PPM 1/4W	18
RM1206 2 KOHM 1% 100 PPM 1/4W	6
RM1206 2.21 KOHM 1% 100 PPM 1/4W	6
RM1206 20 KOHM 1% 100 PPM 1/4W	6
RM1206 221 OHM 1% 100 PPM 1/4W	6
RM1206 27.4 KOHM 1% 100 PPM 1/4W	2
RM1206 332 OHM 1% 100 PPM 1/4W	12
RM1206 4.02 KOHM 1% 100 PPM 1/4W	18
RM1206 4.75 KOHM 1% 100 PPM 1/4W	6
RM1206 47.5 KOHM 1% 100 PPM 1/4W	14
RM1206 5.11 KOHM 1% 100 PPM 1/4W	8
RM1206 5.62 KOHM 1% 100 PPM 1/4W	18
RM1206 51.1 KOHM 1% 100 PPM 1/4W	8
RM1206 52.3 KOHM 1% 100 PPM 1/4W	6
RM1206 9.31 KOHM 1% 100 PPM 1/4W	4
RM1206 93.1 KOHM 1% 100 PPM 1/4W	6
RNC55J 22.1 KOHM 0.1% 1/10W	36
RNC55J 665 KOHM 0.1% 1/10W	3

RNR55E 1.5 KOHM 0.1% 1/10W	2
RNR55E 10 KOHM 0.1% 1/10W	10
RNR55E 15.8 KOHM 0.1% 1/10W	4
RNR55E 165 KOHM 0.1% 1/10W	3
RNR55E 200 KOHM 0.1% 1/10W	4
RNR55E 27.4 KOHM 0.1% 1/10W	2
RNR55E 3.65 KOHM 0.1% 1/10W	2
RWR80N 150 OHM 1% 2W	54
RWR80N 2.21 KOHM 1% 2W	14
2N2907-SMD	20
2N3700-SMD	22

Table 1.17: Components List - MVL card

13.4. Name of Design: Bus bar

a. Brief Description/functionality of module:

The proposed Power Conditioning Unit (PCU) features the power bus formation inside the package. The formed power bus is connected to spacecraft distribution bus bar. The bus bar module contains the bus bar which facilitate the connection of formed bus bar inside the package to the distribution bus bar. As whole of the spacecraft load current pass through these bus bar, the Load Current Sensors (LCS) sensing unit is accommodated along with these bus bar.

13.5. Name of the design: Boost Shunt Regulator (BSR)

S.No	Parameters	Remarks
1	Name of Design	Boost Shunt Regulator (BSR)
2	Brief Description/functionality of module	Boost shunt regulator is a Pulse Width Modulator based current fed boost converter with solar array as the input and bus as its output. It keeps the solar array voltage fixed and eliminates the array switching from zero voltage to Bus voltage.

2a	Block diagram	SA Bypass Bus_Live Str. Boost Bus_Live Boost Bus_Live Bus_Enve Fig: 1.8 Block diagram- Boost shunt regulator
2b	Powering scheme	Input is Solar Array Simulator & Output is the BUS. Before Powering On, ensure load current is greater than string current capacity.
2c	Grounding scheme	Signal ground and Bus RTN shall be connected externally.
2d	Power handling and dissipation	BSR handles 100V @ 12A i.e. 1200W power with a dissipation of 30W.
2e	No of modules	Three (03).
2f	Interface Details	It needs MVL signal for regulating the Bus. It gives string voltage as analog telemetry. A 5V level command can be exercised under the failure and load demand conditions.
2g	Input/ output Information	Input is Solar Array Simulator & Output is the BUS.
3	Component List	Summary of active & passive elements (type/style/Qty): Mentioned separately

Table 1.18: Design details – Boost shunt Regulator modules

Component List

TYPE	PART NO	PACKAGE	QUANTITY
ICS	78845A-DIP8	DIP8	2
ICS	4093B-CFP14	CFP14	2
ICS	111-TO99	ТО99	2
ICS	4049UB-CFP16	CFP16	1
ICS	78845A-CFP8	CFP8	1
ICS	2941-SOP16	SOP16	1

ICS	1708-DIP8	DIP8	2
ICS	124-SOP14	SOP14	1
DIO	1N4625-SMD	SMD	4
DIO	1N6328-DO35	DO7/DO35	5
DIO	1N4569-SMD	SMD	4
DIO	1N4627-SMD	SMD	2
DIO	HFB16HY20C-TO257	TO257	8
DIO	1N6642-SMD	SMD	10
DIO	1N5806-SMD	SMD	12
DIO	1N5811-SMD	SMD	5
DIO	1N5822-SMD	SMD	8
TRA	NEW-2N7586-TO254AA	TO254AA	5
TRA	2N3019-TO5	TO5/TO39	2
TRA	2N5666-TO5	TO5/TO39	1
RES	RER75 1.5 OHM 1% 30W	RER75	2
RES	RLR07 33 KOHM 2% 1/4W	RCR07	4
RES	RM1206 16.2 OHM 1% 100 PPM 1/4W	RM1206	7
RES	RM1206 9.09 KOHM 1% 100 PPM 1/4W	RM1206	4
RES	RM1206 12.1 KOHM 1% 100 PPM 1/4W	RM1206	35
RES	RM1206 1.21 KOHM 1% 100 PPM 1/4W	RM1206	2
RES	RM1206 150 KOHM 1% 100 PPM 1/4W	RM1206	2
RES	RM1206 6.81 KOHM 1% 100 PPM 1/4W	RM1206	4
RES	RWR80N 274 OHM 1% 2W	RWR80	6
RES	RM1206 10 OHM 1% 100 PPM 1/4W	RM1206	2
RES	RM1206 22.1 KOHM 1% 100 PPM 1/4W	RM1206	2
RES	RM1206 17.4 KOHM 1% 100 PPM 1/4W	RM1206	2
RES	RM1206 35.7 KOHM 1% 100 PPM 1/4W	RM1206	6
RES	RM1206 4.75 KOHM 1% 100 PPM 1/4W	RM1206	2
RES	RM1206 15 KOHM 1% 100 PPM 1/4W	RM1206	12
RES	RWR80N 332 OHM 1% 2W	RWR80	12
RES	RM1206 3.32 KOHM 1% 100 PPM 1/4W	RM1206	6
RES	RNR55E 11.7 KOHM 0.1% 1/10W	RNC55	1
RES	RNR55E 2.7 KOHM 0.1% 1/10W	RNC55	1
RES	RNR55E 56.2 KOHM 0.1% 1/10W	RNC55	1
RES	RM1206 100 KOHM 1% 100 PPM 1/4W	RM1206	4
RES	RM1206 47.5 KOHM 1% 100 PPM 1/4W	RM1206	2
RES	RM1206 475 KOHM 1% 100 PPM 1/4W	RM1206	1
RES	RM1206 5.62 KOHM 1% 100 PPM 1/4W	RM1206	5
RES	RM1206 56.2 KOHM 1% 100 PPM 1/4W	RM1206	1
RES	RM1206 1 KOHM 1% 100 PPM 1/4W	RM1206	4
RES	RM1206 33.2 KOHM 1% 100 PPM 1/4W	RM1206	1
RES	RWR80N 6.04 OHM 1% 2W	RWR80	1
RES	RM1206 27.4 KOHM 1% 100 PPM 1/4W	RM1206	2
RES	RWR80S 2.21 KOHM 1% 2W	RWR80	6
RES	RM1206 5.11 KOHM 1% 100 PPM 1/4W	RM1206	5
RES	RM1206 1.5 KOHM 1% 100 PPM 1/4W	RM1206	1

RES	RM1206 2.21 KOHM 1% 100 PPM 1/4W	RM1206	1
RES	RWR80N 1 OHM 1% 2W	RWR80	1
RES	RNR55E 750 OHM 0.1% 1/10W	RNC55	1
RES	RM1206 3.92 KOHM 1% 100 PPM 1/4W	RM1206	1
RES	RM1206 2 KOHM 1% 100 PPM 1/4W	RM1206	4
RES	RM1206 8.66 KOHM 1% 100 PPM 1/4W	RM1206	1
RES	RM1206 48.7 KOHM 1% 100 PPM 1/4W	RM1206	7
CAP	NEW-PM948NS-4 4.7UF 10% 200V -NA	NA	4
CAP	NEW-PM948NS-4 8.2UF 10% 170V-NA	NA	10
CAP	CKR06 10 KPF 10% 200V	CKR06	10
CAP	CDR34 0.18 UF +/-10% TC+15%-25% 50V	CDR34	18
CAP	CDR32 470 PF +/-1% 30 PPM 100V	CDR32	4
CAP	CDR35 0.22 UF +/-10% TC +15%-25% 50V	CDR35	2
CAP	CDR33 1 KPF +/-10% 30 PPM 100V	CDR33	2
CAP	CKR06 0.1 UF 10% 100V	CKR06	2
CAP	CDR33 2.2 KPF 1% 30 PPM 100V	CDR33	2
CAP	CDR31 220 PF +/-1% 30 PPM 100V	CDR31	1
CAP	MLCC2225 1.2 UF 10% TC +15%-15% 200V	MLCC2225	7
CAP	CDR34 27 KPF +/-10% TC +15%-25% 100V	CDR34	2
CAP	MLCC2225 2.2 UF +/-5% TC +15%-15% 50V	MLCC2225	17
CAP	CWR29 4.7 UF 5% 50V SNPB-CASEH	CWR29-H	6
CAP	CKR06 0.56 UF 10% 50V	CKR06	4
CAP	CWR29 15 UF 5% 35V SNPB-CASEX	CWR29-X	2
COR	58109-A2	NA	1
COR	55410-W4	NA	1
COR	YP-40705-TC	NA	2
COR	55287-M4	NA	1
FUS	FM12A-15A-135V-RADIAL	RADIAL	3
FUS	FM12A-5A-135V-RADIAL	RADIAL	1

Table 1.19: Components list - Boost shunt Regulator module

13.6. Name of the design: DECODER

S.No	Parameters	Remarks
1	Name of Design	DECODER
2	Brief Description/functionality of module	The requirement of commanding is very high in this system hence a separate decoder circuit is planned. The FPGA card generates the necessary control signals to those card to decode the command pulse of level commands. The 5V commands are distributed directly or some case converted to 28V commands with high current drive support and distributed.
2a	Block diagram	
2b	Powering scheme	Domestic Regulator+ 6.1±0.3V: ~20mASpecifications+ 24±0.3V: Pulse

		estimated 50mA
2c	Grounding scheme	DSPG scheme for 5V & 24V commands
2d	Power handling and dissipation	There are no high dissipating components in the PCB. The maximum estimation in complete PCB will be about Pulsed ~1W
2e	No of modules	1
2f	Interface Details	5V /24V interface to Relays
3	Component List	Summary of active & passive elements (type/style/Qty): Mentioned below

Table 1.20: Design Details – Decoder card/ module

COMPONENT LIST:

SI. No.	Component Details	Package	Quantity
ICS			
1	High Side Relay Driver HMC	CFP44	5
2	UCDA ASIC (URSC Supplied)	CQFP256	2
3	CD4050-CFP16	CFP16	2
4	CD40106B-CFP14	CFP14	2
5	GP250-720-EDB-26V-L-CAN2	CAN2	2
6	TPS7H4501-SP	CFP16	2
7	TPS7H2201-SP	CFP16	2
8	1N6642-SMD	DO213AA	100
9	1N5806-SMD	D5A	4
10	CDR33 0.1 UF +/-10% TC +15%-25% 50V	CDR33	28
11	RM0505 1 KOHM 1% 100 PPM 1/20W	RM0505	30
12	RM0505 10 KOHM 1% 100 PPM 1/20W	RM0505	30
13	RM0505 100 KOHM 1% 100 PPM 1/20W	RM0505	30
14	DSUBN-50P-PCB-90L5	-	2
15	FRB-144-ML	-	1

Table 1.21: Components List – Decoder card/ module

13.7. NAME OF DESIGN: FPGA CARD

S.No	Parameters	Remarks
1	Name of Design	FPGA CARD
2	Brief	The requirement of commanding is very high in this
	Description/functionality	system hence a separate decoder card is planned.
	of module	The FPGA card generates the necessary control
		signals to those card to decode the command pulse
		of level commands. The 5V commands are
		distributed directly or some case converted to 28V
		commands with high current drive support and
		distributed.

2a	Block diagram	Analog TMs Digital TMs Digital TMs Fig: 1.9: Block diagram	ADC FPGA Control Signals Commands MDC FPGA Commands Commands Commands
2b	Powering scheme	Domestic Regulator Specifications estimated Derived Voltages for Digital devices Voltages for Analog devices	+14.7±0.5V: ~20mA -14.7±0.5V : ~10mA + 6.1±0.3V: ~250-300mA, ~1.2A pulsed 2ms for every 1s 5V, 3.3V and 1.5V ±14V, 5.6V and 3.3V (Derived)
2c	Grounding scheme	DSPG scheme Short Analog Ground and Digital Ground at ADC end and connect same to CHASIS through low impedance planes.	
2d	Power handling and dissipation	There are no high dissipating components in the PCB. The maximum estimation in complete PCB will be about 3.5W	
2e	No of modules	2	
2f	Stacking of modules/stacking diagram		
2g	Interface Details	1553 interface for signal interface 0-3 modules.	external communication and 5V analog /digital between
2h	Input/ output Information		
3	Component List	Refer below section	

Table 1.22: Design Details – FPGA Card

Details for SI. No. 3 above: Component List

TYPE	PART NO.	QTY
CAP	CDR31 1 KPF +/-10% TC +15%-25% 100V	8

CAP	CDR31 10 KPF +/-10% TC +15%-25% 50V	20
CAP	CDR31 150 PF +/-1% 30 PPM 100V	2
CAP	CDR32 6.8 KPF +/-10% TC +15%-25% 100V	1
CAP	CDR33 0.1 UF +/-10% TC +15%-25% 50V	62
CAP	CDR33 22 KPF +/-10% TC +15%-25% 100V	8
CAP	CDR35 0.22 UF +/-10% TC +15%-25% 50V	1
CAP	CDR35 0.47 UF +/-10% TC +15%-25% 50V	4
CAP	CWR29 10 UF 5% 35V SNPB-CASEH	2
CAP	CWR29 33 UF 5% 15V SNPB-CASEH	7
CAP	CWR29 47 UF 5% 10V SNPB-CASEH	1
DIO	1N4569-SMD	2
DIO	1N4627-SMD	8
DIO	1N5806-SMD	6
DIO	1N5822-SMD	2
DIO	1N6642-SMD	46
HMC	09C102L-SIP9	2
HMC	09C103L-SIP9	2
HMC	09C104L-SIP9	4
HMC	09C223L-SIP9	4
HMC	09C472L-SIP9	2
HMC	09C474L-SIP9	10
ICS	124-SOP14	8
ICS	128S102-FPWG16	1
ICS	136-2.5V-TO46	1
ICS	238A790-211T-CFP28	2
ICS	4050-5V-SOP10	1
ICS	43-CFP10	2
ICS	54ACTQ16244-CFP48	6
ICS	54HC14-CFP14	1
ICS	54LVTH162244-CFP48	2
ICS	7A4501-MBCFP10	4
ICS	BU67402F80KL-431Z-MBCFP36	1
ICS	RTAX2000S-CQFP352	1
OSC	OSC-24MH3.3VHCMOS-SMD4	1
REL	GP250-720-E00-26V-L-CAN2	1
RES	RM0505 1 KOHM 1% 100 PPM 1/8W	104
RES	RM0505 1.5 KOHM 1% 100 PPM 1/8W	8
RES	RM0505 10 KOHM 1% 100 PPM 1/8W	36
RES	RM0505 100 KOHM 0.1% 100 PPM 1/8W	7
RES	RM0505 100 KOHM 1% 100 PPM 1/8W	2
RES	RM0505 15 KOHM 1% 100 PPM 1/8W	1
RES	RM0505 15.4 KOHM 1% 100 PPM 1/8W	1
RES	RM0505 162 OHM 1% 100 PPM 1/8W	1
RES	RM0505 221 KOHM 1% 100 PPM 1/8W	1
RES	RM0505 3.01 KOHM 1% 100 PPM 1/8W	8
RES	RM0505 30.1 KOHM 1% 100 PPM 1/8W	2

RES	RM0505 33.2 KOHM 1% 100 PPM 1/8W	1
RES	RM0505 47.5 KOHM 1% 100 PPM 1/8W	1
RES	RM0505 5.11 KOHM 1% 100 PPM 1/8W	1
RES	RM0505 5.62 KOHM 1% 100 PPM 1/8W	9
RES	RM0505 5.76 KOHM 1% 100 PPM 1/8W	2
RES	RM0505 562 OHM 1% 100 PPM 1/8W	14
RES	RM0505 750 KOHM 1% 100 PPM 1/8W	2
RES	RM0505 90.9 OHM 1% 100 PPM 1/8W	4
RES	RM1206 1 KOHM 1% 100 PPM 1/4W	12
RES	RM1206 1.74 KOHM 1% 100 PPM 1/4W	6
RES	RM1206 10 KOHM 1% 100 PPM 1/4W	8
RES	RM1206 12.1 KOHM 1% 100 PPM 1/4W	2
RES	RM1206 14.7 KOHM 1% 100 PPM 1/4W	2
RES	RM1206 16.5 KOHM 1% 100 PPM 1/4W	2
RES	RM1206 18.2 KOHM 1% 100 PPM 1/4W	8
RES	RM1206 19.6 KOHM 1% 100 PPM 1/4W	1
RES	RM1206 20 KOHM 1% 100 PPM 1/4W	6
RES	RM1206 22.1 KOHM 1% 100 PPM 1/4W	4
RES	RM1206 249 OHM 1% 100 PPM 1/4W	4
RES	RM1206 33.2 KOHM 1% 100 PPM 1/4W	10
RES	RM1206 4.75 KOHM 1% 100 PPM 1/4W	4
RES	RM1206 470 OHM 1% 100 PPM 1/4W	1
RES	RM1206 5.62 KOHM 1% 100 PPM 1/4W	7
RES	RM1206 681 OHM 1% 100 PPM 1/4W	2
RES	RWR80N 200 OHM 1% 2W	4
RES	RWR80N 221 OHM 1% 2W	16
TRA	2N2907-SMD	1
TRA	2N3700-SMD	1
TRA	66168-TO78	2
ICS	TPS7H2201-SP	1
CORE	SRFB1206-601	5
ICS	4050-2.5V-SOP10	1

Table 1.23: Component List - FPGA card

13.8. Name of the design: DOMESTIC REGULATOR

The vendor shall design and realise the dc-dc converter as per the specification given with necessary protection scheme(Built to spec)

a. SPECIFICATIONS:

Domestic regulator Module consists two numbers of DC-DC converter(main & redundant) which should have output voltages capable of supporting all the power electronics circuits mentioned above

SPECIFICATIONS

	Outputs	Specifications
1.	Output-1	+14.7V/3500 mA
2.	Output-2	-14.7V/1700 mA
3.	Output-3	12.7V/500 mA
4.	Output-4	6.0 V/800 mA
5.	Output-5	24.0 V/150mA
6.	Max. Output Power per Dom- regulator	85W
7.	EMI/EMC Compliance	MIL-461G/URSC Standard

Table 1.24: Specifications – Domestic Regulator

b. PROTECTION SCHEME:

• Dom-reg Over load/short circuit protection feature for all the outputs

13.9. NAME OF THE DESIGN: BATTERY CURRENT SENSOR (BCS)

1	Name of Design	BCS
2	Brief Description/functionality of module	The battery current sensor (BCS) will be a non- contact magnetic based current sensor.Battery current sensor (BCS) provides the charge and discharge current passing through the battery.
2a	Block diagram	Fig: 1.10: Block diagram: Bat. Current sensor
2b	Powering scheme	Powered with +/-14V
2c	Grounding scheme	DSPG
2d	Power handling and dissipation	<200mA &<1W
2e	No of modules	2
2f	Stacking of modules/stacking diagram	Part of battery module
2g	Interface Details	0 to 5V interface to core power FPGA
2h	Input/ output Information	Input: 50A Charge & 190A discharge

		Output: charge & discharge with 2 ranges -50A(charge) to 190A(discharge) Total 4 ranges with 0 to 5V
3	Component List	Summary of active & passive elements (type/style/Qty): Mentioned below

Table 1.25: Design details – Battery current Sensor

Details for serial No.3 above: Component List (for one Module)

PART NO	QTY.
CDR31 1 KPF +/-10% TC +15%-25% 100V	3
CDR31 10 KPF +/-10% TC +15%-25% 50V	4
CDR33 0.1 UF +/-10% TC +15%-25% 50V	23
CDR33 1 KPF +/-1% 30 PPM 100V	1
CDR33 22 KPF +/-10% TC +15%-25% 100V	4
CWR29 22 UF 5% 25V SNPB-CASEG	2
CWR29 4.7 UF 5% 50V SNPB-CASEH	2
DSUBN-25S-PCB-90L5	1
DSUBN-9P-PCB-90L5	1
1N4100-SMD	1
1N4103-SMD	1
1N4569-SMD	1
1N5806-SMD	4
1N6642-SMD	4
FM12A-5A-135V-RADIAL	2
117-TO39	1
124-SOP14	3
139-CFP14	2
4013B-CFP14	1
585-DIP14	1
RM0505 1 KOHM 1% 100 PPM 1/8W	1
RM0505 10 KOHM 1% 100 PPM 1/8W	11
RM0505 100 KOHM 1% 100 PPM 1/8W	1
RM0505 20 KOHM 1% 100 PPM 1/8W	5
RM0505 6.81 KOHM 1% 100 PPM 1/8W	2
RM0505 9.09 KOHM 1% 100 PPM 1/8W	1
RM1206 1 KOHM 1% 100 PPM 1/4W	5
RM1206 1.43 KOHM 1% 100 PPM 1/4W	1
RM1206 11.2 KOHM 1% 100 PPM 1/4W	1
RM1206 18.2 KOHM 0.1% 100 PPM 1/4W	4
RM1206 200 KOHM 1% 100 PPM 1/4W	3
RM1206 22.1 KOHM 1% 100 PPM 1/4W	4
RM1206 221 KOHM 0.1% 100 PPM 1/4W	1
RM1206 4.75 KOHM 1% 100 PPM 1/4W	1
RM1206 5.11 KOHM 1% 100 PPM 1/4W	2

RM1206 732 OHM 1% 100 PPM 1/4W	1
RM1206 8.25 KOHM 1% 100 PPM 1/4W	1
RM1206 82.5 KOHM 1% 100 PPM 1/4W	1
RM1206 9.09 KOHM 0.1% 100 PPM 1/4W	2
RM1206 9.09 KOHM 1% 100 PPM 1/4W	1
RWR80N 200 OHM 1% 2W	4
RWR80N 56.2 OHM 1% 2W	6
2N3700-SMD	1
2N7261-TO39	2
2N7389-TO39	2
52315	2

Table 1.26: Component List – Battery current Sensor

S.N	Parameters	Remarks
0		
1	Name of Design	LCS
2	Brief Description/functionalit y of module	The load current sensor (LCS) will be a non-contact magnetic based current sensor. Load current passing through the bus bar is measured and various ranges of output values are generated. Also houses circuit required for battery dumping.
2a	Block diagram	POWER LIVE RETURN LCS LCS DUMP CARD
		$\stackrel{\downarrow}{=}_{T_{-}}^{*} \stackrel{\text{BAT-1}}{\longrightarrow} \stackrel{\text{A}}{\longrightarrow} \stackrel{\text{A}}{\longrightarrow} \stackrel{\text{I}}{\longrightarrow} \stackrel{\text{I}}$
2b	Powering scheme	Powered with +/-14V from dom.reg

13.10. NAME OF THE DESIGN: LCS

2c	Grounding scheme	DSPG
2d	Power handling and	<200mA &<200mW
	dissipation	
2e	No of modules	2
2f	Stacking of modules/stacking diagram	Part of core power packagebus bar module
2g	Interface Details	0 to 5V interface to core power FPGA
2h	Input/output	
	input/output	Input. 0 to 250A
	Information	Output: 4 ranges with 0 to 5V
3	Information Component List	Output: 4 ranges with 0 to 5V Summary of active & passive elements (

Table 1.27: Design details – Load current Sensor

Details for SI. No. 3 above: COMPONENT LIST (FOR ONE MODULE)

PART NO	QTY
CDR31 1 KPF +/-10% TC +15%-25% 100V	1
CDR31 10 KPF +/-10% TC +15%-25% 50V	1
CDR33 0.1 UF +/-10% TC +15%-25% 50V	23
CDR33 1 KPF +/-1% 30 PPM 100V	3
CWR29 22 UF 5% 25V SNPB-CASEG	2
DSUBN-15S-PCB-90L5	1
DSUBN-25P-PCB-90L5	1
1N4569-SMD	1
1N4624-SMD	4
1N4626-SMD	1
1N5806-SMD	7
1N6642-SMD	2
FM12A-5A-135V-RADIAL	2
117-TO39	1
124-SOP14	2
139-CFP14	1
585-DIP14	1
RM0505 10 KOHM 1% 100 PPM 1/8W	2
RM0505 11 KOHM 1% 100 PPM 1/8W	1
RM0505 121 KOHM 1% 100 PPM 1/8W	1
RM0505 20 KOHM 1% 100 PPM 1/8W	1
RM1206 1 KOHM 1% 100 PPM 1/4W	6
RM1206 1.43 KOHM 1% 100 PPM 1/4W	1
RM1206 1.5 KOHM 1% 100 PPM 1/4W	1
RM1206 10 KOHM 1% 100 PPM 1/4W	10
RM1206 11.2 KOHM 1% 100 PPM 1/4W	1
RM1206 18.2 KOHM 0.1% 100 PPM 1/4W	4

RM1206 22.1 KOHM 1% 100 PPM 1/4W	6
RM1206 24.3 KOHM 1% 100 PPM 1/4W	4
RM1206 243 KOHM 0.1% 100 PPM 1/4W	4
RM1206 6.81 KOHM 1% 100 PPM 1/4W	3
RM1206 64.9 KOHM 1% 100 PPM 1/4W	8
RM1206 8.25 KOHM 1% 100 PPM 1/4W	2
RWR80N 221 OHM 1% 2W	7
RWR80N 43.2 OHM 1% 2W	4
2N3501-SMD	4
2N3700-SMD	1
2N5666-TO5	2
2N7389-TO39	1
2N7549-TO254	4

Table 1.28: Components List – Load current Sensor

13.11. NAME OF THE DESIGN: BCR

S.No	Parameters	Remarks
1	Name of Design	BCR
2	Brief Description/functionality of	Battery Charge Regulator:
	module	Mentioned below
2a	Block diagram	Attached
2b	Powering scheme	Attached
2c	Grounding scheme	Attached
2d	Power handling and dissipation	1000W / 40W
2e	No of modules	3
2f	Stacking of modules/stacking	
	diagram	
2g	Interface Details	Interface with FPGA
2h	Input/ output Information	
		Bus input and battery output
3	Component List	Mentioned below

Table 1.29: Design details – Battery Charge regulator

Details for SI. No. 2 . DESCRIPTION OF THE HARDWARE:

The battery charge regulator (BCR) is designed to charge Li-Ion battery directly from 100V BUS. BCR, which is essentially a non-isolated buck (step down) dc-dc converter, is designed to charge a lower voltage battery from a higher voltage bus. It is capable of charging battery with CC-CV as shown in Figure 2. It can charge Li-Ion battery with regulated constant current until End of Charge (EOC) voltage is reached. These current and EOC voltage set points can be selected using 16-bit tele-command to 256 different levels each. It can be switched ON/OFF by tele-

command and has in-built over-current protection and FPGA interface for over-voltage protection.

Details for SI. No.2: BLOCK DIAGRAM



Fig. 1.12 Block diagram BCR



Fig. 1.13 BCR Grounding Scheme:

Details for SI. No. 3 above: Components list:

TYPE	PART NO.	QTY
CAP	CDR31 10 PF +/-1% 30 PPM 100V	2
CAP	CDR31 220 PF +/-1% 30 PPM 100V	1
CAP	CDR32 330 PF +/-1% 30 PPM 100V	4
CAP	CDR32 4.7 KPF +/-10% TC +15%-25% 100V	1
CAP	CDR32 5.6 KPF +/-10% TC +15%-25% 100V	1
CAP	CDR32 6.8 KPF +/-10% TC +15%-25% 100V	1
CAP	CDR33 0.1 UF +/-10% TC +15%-25% 50V	45
CAP	CDR33 1 KPF +/-5% 30 PPM 100V	1
CAP	CDR33 22 KPF +/-10% TC +15%-25% 100V	1
CAP	CDR33BXU 0.1 UF +/-10% TC+15%-25% 100V	2
CAP	CDR35 0.22 UF +/-10% TC +15%-25% 50V	2

CAP	CDR35 0.47 UF +/-10% TC +15%-25% 50V	8
CAP	CLR79 86 UF 10% 100V	6
CAP	CWR29 10 UF 10% 35V SNPB-CASEH	1
CAP	CWR29 10 UF 5% 35V SNPB-CASEH	1
CAP	MLCC1206 47 KPF 10% 200V	4
CAP	MLCC2220 2.2 UF +/-10% TC +15%-15% 100V	1
CON	DSUB-COMBO-POWER-5W5M-90	1
COR	58349-A2	3
COR	YP-40907-TC	5
DIO	1N4569-SMD	2
DIO	1N5806-SMD	18
DIO	1N5811-SMD	1
DIO	1N5822-SMD	8
DIO	1N6642-SMD	26
DIO	35CGQ150-TO254	6
FUS	FM12A-15A-135V-RADIAL	6
ICS	07-TO99	3
ICS	124-SOP14	3
ICS	139-CFP14	1
ICS	1825-CFP16	1
ICS	40106B-CFP14	2
ICS	4071B-CFP14	1
ICS	4094B-CFP16	2
ICS	4424-MBCFP16	2
ICS	565-CFP24	2
ICS	8212-CFP10	1
REL	GP250-720-E00-26V-L-CAN2	2
RES	CS303145 0.005 OHM 0.5% 25 PPM 3W	1
RES	RM0505 1 KOHM 1% 100 PPM 1/8W	13
RES	RM0505 1.21 KOHM 1% 100 PPM 1/8W	1
RES	RM0505 10 KOHM 1% 100 PPM 1/8W	2
RES	RM0505 10 KOHM 5% 100 PPM 1/20W	17
RES	RM0505 100 KOHM 1% 100 PPM 1/8W	6
RES	RM0505 18.2 KOHM 1% 100 PPM 1/20W	4
RES	RM0505 2.55 KOHM 1% 100 PPM 1/20W	2
RES	RM0505 221 OHM 1% 100 PPM 1/8W	2
RES	RM0505 274 OHM 1% 100 PPM 1/8W	2
RES	RM0505 3.92 KOHM 1% 100 PPM 1/8W	2
RES	RM0505 33.2 KOHM 1% 100 PPM 1/8W	2

RES	RM0505 4.32 KOHM 1% 100 PPM 1/20W	1
RES	RM0505 4.75 KOHM 1% 100 PPM 1/8W	1
RES	RM0505 750 KOHM 1% 100 PPM 1/20W	6
RES	RM0505 9.31 KOHM 1% 100 PPM 1/8W	1
RES	RM1206 1 KOHM 1% 100 PPM 1/4W	2
RES	RM1206 10 KOHM 1% 100 PPM 1/4W	29
RES	RM1206 10 OHM 1% 100 PPM 1/4W	2
RES	RM1206 100 KOHM 1% 100 PPM 1/4W	2
RES	RM1206 121 KOHM 1% 100 PPM 1/4W	1
RES	RM1206 121 OHM 1% 100 PPM 1/4W	8
RES	RM1206 13.3 KOHM 1% 100 PPM 1/4W	1
RES	RM1206 15 KOHM 1% 100 PPM 1/4W	2
RES	RM1206 150 KOHM 1% 100 PPM 1/4W	4
RES	RM1206 2 KOHM 1% 100 PPM 1/4W	1
RES	RM1206 20 KOHM 1% 100 PPM 1/4W	2
RES	RM1206 3.32 KOHM 1% 100 PPM 1/4W	1
RES	RM1206 3.92 KOHM 1% 100 PPM 1/4W	2
RES	RM1206 4.75 KOHM 1% 100 PPM 1/4W	5
RES	RM1206 4.99 KOHM 1% 100 PPM 1/4W	1
RES	RM1206 422 OHM 1% 100 PPM 1/4W	1
RES	RM1206 6.81 KOHM 1% 100 PPM 1/4W	4
RES	RM1206 60.4 KOHM 1% 100 PPM 1/4W	4
RES	RM1206 604 OHM 1% 100 PPM 1/4W	5
RES	RM1206 7.5 KOHM 1% 100 PPM 1/4W	1
RES	RM1206 75 KOHM 0.1% 100 PPM 1/4W	1
RES	RNR55E 10 KOHM 0.1% 1/10W	4
RES	RNR55E 14 KOHM 0.1% 1/10W	1
RES	RNR55E 2 KOHM 0.1% 1/10W	1
RES	RNR55E 34.8 KOHM 0.1% 1/10W	1
RES	RNR55e 42.2 kohm 0.1% 1/10w	4
RES	RNR55E 6.04 KOHM 0.1% 1/10W	1
RES	RNR55E 75 KOHM 0.1% 1/10W	1
RES	RWR80N 100 OHM 1% 2W	5
RES	RWR80N 150 OHM 1% 2W	2
RES	RWR80N 221 OHM 1% 2W	18
RES	RWR80N 30.1 OHM 1% 2W	2
TRA	2N2905-TO39	4
TRA	2N2907-SMD	4
TRA	2N3637-SMD	3

TRA	2N3700-SMD	5
TRA	2N5666-TO5	2
TRA	NEW-BUY25CS45B-TO254	4
TRA	NEW- IRHMS9A7264 (ALTERNATE ON/OFF NMOS)	2
TRA	NEW-597260-TO254	4
FUS	NEW-FM13-1/4A SMD	2
CAP	NEW-PM-948 /170V/8.2 UF	12
CON	NEW-44PIN-MOTHERBOARD CONN	1
TRA	2N7269-TO254 (ALTERNATE SWITCHER MOSFET)	4

Table 1.30: Component List – Battery Charge regulator

13.12. NAME OF THE DESIGN: ICM

1.	Name of Design	ICM
2.	Brief Description/functionality of module	Individual Cell Monitoring (ICM) card processes the cell voltage inputs from each battery cell and converts into analog voltage TMs that will be used for cell voltage monitoring, Under voltage protection logic and Over Charge protection logics. Battery voltage monitoring circuit processes battery voltage to analog TM output which will be used for charge/discharge control of onboard battery. Apart from these two functionalities ICM card also has thermistor interfaces from battery, monitoring resistors for ground monitoring and fused battery sense lines for other bus control modules.

2a	Block diagram	+12V -12V		
		Battery Voltage to GC U/P		
		Battery thermistor I/P Battery Sense +ve I/P Battery Sense +ve I/P Battery Sense +ve O/P Battery Sense +ve O/P		
		AMUX AMUX AMUX AMUX		
		Address from FPGA card		
		→ Bottery Sense -ve O/P		
		Fig. 1.14 Block Diagram: ICM		
2b	Powering scheme	Powered by bias DC-DC(+/- 12V)		
2c	Grounding scheme	DSPG		
2d	Power handling and	<500mW dissipation		
	dissipation			
2e	No of modules	3		
2f	Stacking of	Part of Battery Module		
	modules/stacking diagram			
2g	Interface Details	+/-10V interface to core power FPGA		
2h	Input/ output Information	Inputs:		
		Cell voltage inputs, battery voltage sense input to		
		BVM, GC and other power modules, battery		
		thermistor inputs.		
		Cell Input range: 2.5V to 4.3V		
		Battery voltage range is: 57.5V to 98.9V		
		Outputs:		
		Telemetry outputs of +/- 10V to FPGA card.		
3	Component List	Summary of active & passive elements		
		(type/style/Qty): Mentioned below		

Table 1.31: Design details - ICM

Details for SI. No. 3 above: Component list:

PART No.	QTY.
CDR01 470 PF +/-10% TC +15%-25% 100V	2
CDR33 0.1 UF +/-10% TC +15%-25% 50V	38
DSUBH-26P-PCB-90L5	2
DSUBN-37P-PCB-90L5	1
1N967-DO35	2
1N4625-DO213AA	2

124-SOP14	2
43-CFP10	2
71840-CFP28	2
INA1H94-SP-CFP8	20
RM1206 1 KOHM 1% 100 PPM 1/4W	6
RM1206 10 KOHM 1% 100 PPM 1/4W	2
RM1206 100 KOHM 1% 100 PPM 1/4W	8
RM1206 12.1 KOHM 1% 100 PPM 1/4W	2
RM1206 150 KOHM 0.1% 100 PPM 1/4W	8
RM1206 2.21 KOHM 1% 100 PPM 1/4W	8
RM1206 27.4 KOHM 0.1% 100 PPM 1/4W	4
RM1206 5.11 KOHM 1% 100 PPM 1/4W	4
RM0505 100 OHM 1% 100 PPM 1/8W	9
FM13 0.5A -SMD	4
FM13 125mA-SMD	4

Table 1.32: Component List - ICM

13.13. NAME OF THE DESIGN: SELF BIAS DC-DC CONVERTER – BUILT TO SPEC: PART OF BATTERY MODULE

S.No	Parameters	Remarks		
1	Name of Design	Self bias DC-DC converter (as part of Battery module)		
2	Brief Description/ functionality of module	Three numbers of ICM card (individual cell monitoring) and two numbers of BCS card (Battery current sensors) are located along with battery. This DCDC card powers circuits in ICM and BCS is also housed as part of Battery module. Main and redundant DC-DC circuits needs to be part of single PCB(Discrete) or Two numbers of HMC can be planned		
2a	Block diagram	100V Bus Live Output Live1 100 V Bus Rtn Digital TM bit BIAS DC-DC converter Output Rtn 1,2 Output Live2 Output Live2		
2b	Powering scheme	Powered with 100V Bus		
2c	Grounding scheme	DC-DC converter return to be provided along with Live lines for each output of converter		
2d	Power handling and dissipation	5W and<1.5W		

2e	No of modules	1
2f	Stacking of modules/stacking diagram	Bias converter is part of battery module and stacking diagram of the same will be provided later
2g	Interface Details	 DC- DC PCB / HMC to have interface for 1) Bus input (Live & Return), 2) Output lines to BCS/ICM circuit (L&R) 3) Output voltage TM (Digital TM) 4) Signal return line 5) Input and output need to be implemented through standard connector interface. Two numbers of standard connector one for main & one connector for redundant DC-DC without any interconnections between them.
2h	Input/ output Information	Input: Bus Output voltages/currents: O/P1 (+14V/0.250A) ; O/P2 (-14V/ 0.100 A) Live lines: 2 lines each for +14V and -14V Common return lines :3 numbers are required
3	Drawing/Dimensions	Built to spec for Bias DC-DC – SMT or HMC type as per our mechanical drawing/ dimensions
4	Dimension , wt, volume	 120mm * 110mm*2.2 mm (SMT option -Two DC-DC circuits in single PCB)# 120 mm* 110 mm* 15 mm (HMC option-Two converters to be accommodated in single PCB footprint size)#
5	Load profile	Maximum Output Power per DC-DC converter = 5W Output voltages/currents: O/P1 (+14V/0.250A) O/P2 (-14V/ 0.100 A)
6	Protections	 Over load/short circuit protection feature @>120% of full rated power (5W) DC-DC to be in Hic-up mode Inrush current limiting feature
7	EMI/EMC Compliance	MIL-461G/URSC Standard

Table No. 1.33 Design details of self bias DC-DC converter

Note: PCB and mechanical dimension shall meet the dimension mentioned above, since these PCBs shall be mounted in the Bat. Module.

13.14. NAME OF THE DESIGN : DROVP

S.No	Parameters	Remarks	
1	Name of Design	Domreg Over Voltage Protection (DROVP) PCB	
2	Brief Description/functionality of module	 DROVP PCB is having over voltage protection feature for all five outputs of Domreg. In case of overvoltage in one Domestic regulator (Main or redundant), the output supply of that particular chain will turn OFF and disable the OVP protection of other chain. This PCB is having following features: Current telemetry circuit (for both main & redundant converter) Analog voltage telemetry of output voltages. OVP status of each Domestic regulator. 	
2a	Block diagram	R/B Live Fuse (M) O/P1 Main OVP circuit O/P3 Chain DC-DC (M) O/P4 OVP OVP circuit O/P4 OVP Switch O/P5 OVP Status VTM R/B Return Current CIM R/B Live Fuse (R) O/P1 OVP Status VTM R/B Live Fuse (R) O/P1 OVP Status OVP Status VTM OVP circuit O/P2 OVP Circuit O/P3 O/P3 R/B Return Current CIM Redundant DC-DC (R) O/P2 OVP circuit O/P3 O/P3 OVP circuit O/P4 O/P4 OVP circuit O/P4 O/P5 OVP circuit O/P5 O/P5 OVP circuit O/P4 O/P5 OVP circuit O/P5 O/P5 OVP circuit O/P5 O/P5 OVP circuit O/P5 O/P5 OVP circuit O/P5 O/P5 OVP circuit <td< th=""></td<>	
2b	Powering scheme	Powered with 100V Bus for current telemetry circuit	
2c	Grounding scheme	 Current TM should be wrt chassis. Each converter outputs return to be provided along with Live lines. 	
2d	Power handling and dissipation	Maximum Power Dissipation =5.5W	
2e	No of modules	1	
2f	Stacking of modules/stacking diagram	DROVP PCB will be mounted in DC-DC tray of Core Power Module and stacking diagram will be provided later.	
2g	Interface Details	 DROVP PCB has to be interfaced for Raw Bus (Live & return), Raw Bus Live will go to DC-DC converter through Fuse. Raw Bus return from DC-DC converter will go 	

		 through current sense resistor present in DROVP PCB. Output lines to users (Live & Return) Output Voltage TM(Analog TM) Output OVP status (Digital TM) Raw Bus Current Telemetry (Analog TM) Input and output interface is through standard connector interface (37 pin DSUB ITT connector). Two numbers of standard connectors one for main &another for redundant DC-DC chain without any interconnections between them is used.
2h	Input/ output Information	Input: Bus Live & Return Output: All five outputs from converter after OVP switch, Voltage telemetry, Current telemetry, OVP status
3	Component list	Mentioned below
4.	EMI/EMC Compliance	MIL-461G/URSC Standard

Table: 1.34 Design details - DROVP

COMPONENTS LIST:

PART No.	QTY.
139-CFP14	10
136-2.5V-TO46	10
124-SOP14	2
1N6327US-SMD	10
1N4624-SMD	8
1N4106-SMD	2
2N7550-TO254	6
2N2907-SMD	2
2N7470-TO254	2
2N7389-TO39	2
2N5666-TO5	2
RM1206 9.09 KOHM 1% 100 PPM 1/4W	42
RM0505 51.1 KOHM 1% 100 PPM 1/8W	12
NO CONNECTION-RM1206	16
RM1206 1 KOHM 1% 100 PPM 1/4W	14
RM1206 57.6 KOHM 1% 100 PPM 1/4W	4
RM0505 41.2 KOHM 1% 100 PPM 1/8W	12
RM1206 5.62 KOHM 1% 100 PPM 1/4W	6
RM1206 20 KOHM 1% 100 PPM 1/4W	4
RM1206 33.2 KOHM 1% 100 PPM 1/4W	6
RM1206 47.5 KOHM 1% 100 PPM 1/4W	8
RM1206 2 KOHM 1% 100 PPM 1/4W	2

RM1206 52.3 KOHM 1% 100 PPM 1/4W	2
RM1206 84.5 KOHM 1% 100 PPM 1/4W	2
RM1206 38.3 KOHM 1% 100 PPM 1/4W	4
RM1206 61.9 KOHM 1% 100 PPM 1/4W	2
RM0505 18.2 KOHM 1% 100 PPM 1/8W	12
RM1206 17.4 KOHM 1% 100 PPM 1/4W	2
RM1206 221 OHM 1% 100 PPM 1/4W	2
RM1206 100 OHM 1% 100 PPM 1/4W	2
RM1206 110 KOHM 1% 100 PPM 1/4W	2
RM1206 392 KOHM 1% 100 PPM 1/4W	4
RM1206 7.5 KOHM 1% 100 PPM 1/4W	2
RWR80N 0.1 OHM 1% 2W	4
RM1206 30.1 KOHM 1% 100 PPM 1/4W	6
CDR33 0.1 UF +/-10% TC +15%-25% 50V	79
CDR31 1 KPF +/-10% TC +15%-25% 100V	10
CDR31 10 KPF +/-10% TC +15%-25% 50V	18
NO CONNECTION-CDR33	4
NEW-FM13-SMD	4
DSUBN-37S-CR	2

1.35 Component list - DROVP

13.15 Motherboard configuration:

The motherboard is used to interconnect the power and signal lines between the Core Power Electronics and Power modules. Parallel to serial converters for digital data transmission is to be part of this unit. Any form of interconnection which reduces the wires/harness can be adopted.

14.0 ANNEXURE

ANNEXURE-A ANALYSIS TO BE PERFORMED

Subject: The analysis to be performed for all the circuits/modules of PCU

ANALYSIS TO BE CONDUCTED	STAGE OF ANALYSIS	S/W & STDs.
1. Signal integrity (SI) analysis	PCB level	
2. Power integrity (PI) analysis	PCB level	
3. EMI-EMC analysis	Module and overall PCU level	The S/W and standards to be used for the analysis will be shared
4.PCB and package level thermal analysis in conduction and conduction + radiation modes	Overall PCU level	with the selected vendors.
5.Mechanical analysis a. Structural(vibr./Modal analysis) b. Thermal analysis	Overall PCU level	
6. Reliability prediction	Circuit level and overall PCU level	
7.Failure Mode Effect and , Criticality Analysis (FMECA)	Circuit level	
8. Worst Case Circuit Analysis(WCCA), Monte-carlo analysis and Sensitivity analysis (SA)	Circuit level	
9.De-rating analysis (DA)	Circuit level	
10.Fault Tree Analysis (FTA)	Package level	

ANNEXURE- B

DEVELOPMENT OF AUTOMATED TEST SYSTEM – FOR CARD & PKG LEVEL TESTS OF IMPP FOR 100V BUS

INSTRUCTIONS:

1	Vendor shall develop Automated test system for IMPP for testing different types of modules as per the specification provided by URSC
2	The Automated Test System must be rack mounted type with a width of 19 inch
3	All cabling from modules to terminal boxes and mounting of the connector boxes is the responsibility of the vendor realising ATE.
3	From Terminal Box to back plate connector termination is also the responsibility of the vendor. The back plate connector shall be 50 pin crimpable type.
4	All PXIe modules, chassis and controller must be from single OEM
5	The vender should install all peripheral/ accessories (Like Display, Key board, Mouse, Printer etc) associated with PXI unit.
7	The overall system software must be compatible with the existing software present with URSC, Bangalore
8	It is the vendors' responsibility to ensure compatibility with the existing test system with URSC and test system will be accepted only after testing.
9	The system must have ability to scale to a Real Time OS based ATE in future, which can also be programmed using Lab-VIEW.
10	The system must have ability to augment with FPGA based PXI/PXIe modules for future enhancement and there must be programming support for these in Lab-VIEW.
12	Vendor should develop data logging feature using one channel of 1553 card by configuring Monitor terminal
13	The testing and validation of the test system by URSC is the responsibility of the vendor.
14	The vendor should have at least one software engineer (Must have Lab-VIEW CLD or CLAD certificate) to develop new software requirements, reports and Lab-VIEW code cleaning.

Technical Specification of proposed "PXI Based Test System"

S.No	Description Hardware	Qty/Set
1	PXIe-Controller, 2.8 GHz Quad Core Controller, Win 10 64-bit	1
	(Multilanguage) or higher	
2	16GB RAM or higher (best possible)	1
3	MIL-STD-1553 - 2 Channel (Single Function) PXI MIL-STD-1553	1
	Interface Modules provide bus controller (BC), remote terminal (RT)	
4	LFH Connector to Four MIL-STD-1553 Twinax and One D-Sub, 3'	1

5	PXI- Industrial, 24 DI, 24 DO, Ch-Ch Isolated DIO; 48-Channel, 24 Sink/Source Inputs, 24 Sink/Source Outputs, Channel-Channel Isolated, With programmable power-up states, .	3
6	SCB-100A Noise Rejecting, Shielded I/O Connector Block	3
7	Cable assembly, Type SH100-100-FLEX, 2 m	3
8	PXIe High-Performance 7 1/2 Digit DMM and 1000 V Digitizer Performs voltage, current, resistance, temperature, inductance, capacitance, and frequency/period measurements, as well as diode tests, in PXI systems.	1
9	PXIe 2 Channel Power Supply, 60V, 1A 2-Channel, 60 V, 1 A PXI Programmable Power Supply—The PXIe is a programmable DC power supply with isolated outputs. I	1
10	PXI, 2000V Isolated RS422/485, 4 Port Serial Interface 4-Port, Isolated, RS485/RS422 PXI Serial Interface Module—The PXI is a high-performance industrial interface for high-speed, port-to-port isolated communication with RS485 and RS422 devices.	1
11	PXI- 64-Channel 300V CAT I Multiplexer 32-Channel, 300 V, 2-Wire PXI Multiplexer Switch Module	1
12	TB-2627 Screw Terminal Block	1
13	PXI 196 ch Multiplexer 196-Channel, 1-Wire PXI Multiplexer Switch Module	1
14	LFH200 to 4x50-Pin DSub Switch Cable (CH-CH Twisted),1m	1
15	PXIe 32 channel +- 10V analog input module. 24 bit resolution 5 Ks/s/Ch.	1
16	PXIe 8 channel upto 30V analog input module. 16 bit resolution 250 Ks/s/Ch.	1
	PXIe (100MHz, 1GS/s)- Oscilloscope Module 100MHz, 1GS/s	1
17	PXIe, 18-Slot 3U PXI Express Chassis with Timing and Sync: Option The PXIe features an all-hybrid backplane to meet a wide range of high-performance test and measurement application needs.	1
18	Power Cord, 250V, 10A, India	1
19	X13 GPIB Cable, MicroD25 to Shielded cable/Standard connector, 2M	1
20	18-Slot Chassis Front Rack Mount Kit, Extended Recess	1
21	Windows 10 IoT Enterprise USB Recovery Media for PXI, Multilanguage	1
22	Standard service program for PXI systems	1
23	Aluminium Rack 19"	1
24	Foldable Monitor 17" TFT LCD Console compatible with 19" Rack or Higher	1
	Extra monitor	
25	Wireless Keyboard and Mouse	1

27	Dsub Connector	72
28	Dsub Connector PIN	3500
29	Isolation Transformer	1
30	Harness	1
31	1553- Loom	8
32	2 port stub	2
33	Panel Mount Connectors Crimp type for 1553	4
34	DMM Connector	2
35	Consumables	1
36	Electrical Accessories	1
37	Stickering tag	1
38	cables - 700 ch	1
39	ICM Simulator – Simulation of 24 cells	1
40	APC Smart-UPS RC 3000VA 230V Harsh Environment	1

ANNEXURE-C

Applicable documents /Standards

The following documents shall serve as reference documents/standards for the contract.

Document Identification	Document title		
ISRO-PAX-300	Workmanship Standards for the Fabrication of Electronics Packages.		
ISRO-PAS-207	Storage, Handling and Transportation requirements for Electronics hardware.		
ISRO-PAS-100	Non-Conformance Control Requirement for ISRO Projects.		
ISRO-PAS-201	Failure Reporting, Analysis and Corrective Action system		
ISRO-PAS-203	Procedures and Review Requirements for Major Ground Tests and Ground Test Facilities		
MIL-HDBK-263B	ESD Control Hand Book		
ISRO-ISAC-QAG-MTA-GL-01	Space Electronics Production Assurance Guidelines		
RQEG-PAD-EPAS-DC4	Work Instructions Document for Electronic Assembly Fabrication		
URSC-CMMA-DOC-COMPMAN/01	EEE Component Management document		
ISRO-PAX-304	Test specifications and requirements for multilayer printed circuit boards.		
ISRO-PAS-400	Contamination Control and Cleanliness Requirements		
ISRO-ITecS-EE-002	Derating Guidelines for EEE parts.		
MIL-STD 461C/E/F/G	EMI/EMC test standard		
MIL-STD-2218	thermal design, analysis and test criteria for airborne electronic equipment		
MIL-STD-810H/704	Ability of equipment to withstand environmental conditions over its lifetime		
MIL-HDBK-217 version 2	Reliability prediction of electronic eqipment		
MIL-STD-1629A	Procedure to perform failure mode.		
MIL-STD-882/IEC 61508	System Safety guidelines		
MIL-STD-975M and 1547	Baseline for Standardization of EEE parts		
SAC/SRA/GEN/GDL/CKT-SCH/1.0	Schematic Design guidelines for generation of PCB		

ANNEXURE- D

LIST OF SPECIAL TEST EQUIPMENTS NEEDED*

SL. NO	EQPT NAME	RATINGS	QUA NTITY	REMARKS/MAKE
01	Battery simulator/Bus simulator	120V, 10KW	02	Lambda
02	Solar array simulator**	130V, 20A	10	Digitronics
03	Test system		01	Refer Annexure 3, PXI based NI make, with Lab view S/W front end
04	Electronic load	120V, 10KW	01	I-Tech
05	Electronic load	120V, 5KW	01	I-Tech

*Note: Shall be procured by the vendor and can be billed to URSC

** 130V,5A units shall be procured, which can be paralleled to make 20A current.